Yahoo Group Archive:
PPLL-VFO

These Yahoo Groups messages were archived in WARC format by ArchiveTeam in 2018. This PDF was generated by Digital Library of Amateur Radio & Communications from the WARC files in 2026.

Date span: 2011-02-12 through 2018-06-18

Source WARC: ppll-vfo.zpjiwqO.warc.gz

Source item: https://archive.org/details/yahoo-groups-2018-09-09T01-41-41Z-8c3abe

Messages included in this PDF: 319

Yahoo replaced the domain portions of email addresses with @... in the archived messages. Characters lost in Yahoo's archived text appear as ?.

Messages are presented in ascending Yahoo message-ID order. Gaps indicate records absent from the source WARC or messages omitted from this PDF as spam.

1. It Works!

Yahoo group: PPLL-VFO
Date: 2011-02-12 13:44:22 UTC
From: llgaalaas
Topic: 1 Message: 1

Sure enough, there was a missed solder joint on the pic socket. Once that was fixed, the VFO came up as expected. I have a rubber ducky from my vx-2r on the sma connector. Able to tune the VFO around and listen to it on my K3. It is within 200Hz of the K3.

More adventures ahead as I find a way to apply the VFO to practical use.

Surprised to be the first to post on this group. I hope there will be many more members and many more posts.

Craig did a great job designing these boards and programming the PIC. I commend him for sticking with this project over the many years. It has been fun watching his enthusiasm grow with every new board along the way.

73,
Larry KB0R

2. Re: It Works!

Yahoo group: PPLL-VFO
Date: 2011-02-12 14:39:29 UTC
From: AA0ZZ
Topic: 1 Message: 2

Larry,
Thanks for the good words. A good message to open the group with.

I'm glad you got it working. Yes, it's always fun to see and hear them spring to life.

Have you done the calibration procedure? If not, that will bring the frequency even closer to your K3 reading. (After that you can go ahead and adjust the calibration of the K3 to match the Si570 - ha!)

By the way, I haven't "advertised" this group yet since we haven't started selling the kits yet. Will be soon.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "llgaalaas" <larry@...> wrote:
>
> Sure enough, there was a missed solder joint on the pic socket. Once that was fixed, the VFO came up as expected. I have a rubber ducky from my vx-2r on the sma connector. Able to tune the VFO around and listen to it on my K3. It is within 200Hz of the K3.
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> More adventures ahead as I find a way to apply the VFO to practical use.
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> Surprised to be the first to post on this group. I hope there will be many more members and many more posts.
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> Craig did a great job designing these boards and programming the PIC. I commend him for sticking with this project over the many years. It has been fun watching his enthusiasm grow with every new board along the way.
>
> 73,
> Larry KB0R
>

3. New Kit at Kanga US

Yahoo group: PPLL-VFO
Date: 2011-03-17 03:01:27 UTC
From: Bill Kelsey
Topic: 3 Message: 3

I am pleased to announce that I have a new kit ready to go. Craig - AA0ZZ - has designed an Si570 based vfo/signal generator that will work as a daughter card on the PICEL III, or as a standalone unit with a control board. The Si570 daughtercard is $45, and the control board is $45. If they are purchased at the same time the total cost is $80. Shipping is $5 for one or both in the US. DX locations will be at cost.

The unit works between 10 and 157 MHz with a 1 Hz resolution. I can be used with a Quadrature Sampling Detector on 80 - 10 meters, or with a standard mixer on 30 - 2 meters.

The control board has two push buttons, a rotary encoder, and a 2x16 LCD. The software source code for the 16F88 is available.

More info is available on my web site at:
http://www.kangaus.com/si570_project.htm

and on Craig's web site (includes all documentation, schematics, etc.) at:
http://cbjohn.com/aa0zz/index.html

The kits are packed and ready to go!

--
73 - Bill - N8ET
www.kangaus.com

4. Re: New Kit at Kanga US

Yahoo group: PPLL-VFO
Date: 2011-03-17 12:22:45 UTC
From: AA0ZZ
Topic: 3 Message: 4

Thanks, Bill.

Well, folks, we are finally at the launch pad and I am quite excited about it. Hope you all like these two new kits as much as I do. I am looking forward to some good interchanges here as we get going.

I will be uploading design files and manuals to the "Files" section tonight. In the mean time, you can find them on the Kanga web site or my web site.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, Bill Kelsey <n8et@...> wrote:
>
> I am pleased to announce that I have a new kit ready to go. Craig -
> AA0ZZ - has designed an Si570 based vfo/signal generator that will work
> as a daughter card on the PICEL III, or as a standalone unit with a
> control board. The Si570 daughtercard is $45, and the control board is
> $45. If they are purchased at the same time the total cost is $80.
> Shipping is $5 for one or both in the US. DX locations will be at cost.
>
> The unit works between 10 and 157 MHz with a 1 Hz resolution. I can be
> used with a Quadrature Sampling Detector on 80 - 10 meters, or with a
> standard mixer on 30 - 2 meters.
>
> The control board has two push buttons, a rotary encoder, and a 2x16
> LCD. The software source code for the 16F88 is available.
>
> More info is available on my web site at:
> http://www.kangaus.com/si570_project.htm
>
> and on Craig's web site (includes all documentation, schematics, etc.)
> at:
> http://cbjohn.com/aa0zz/index.html
>
> The kits are packed and ready to go!
>
> --
> 73 - Bill - N8ET
> www.kangaus.com
>

5. Use with the PIC-EL, version 1

Yahoo group: PPLL-VFO
Date: 2011-03-18 01:30:10 UTC
From: wb8icn
Topic: 5 Message: 5

I bought the first version of the PIC-EL and really like. The question is will it work with the PPLL-VFO. I read that is does work with version three.

...Mikey, WB8ICN

6. Re: Use with the PIC-EL, version 1

Yahoo group: PPLL-VFO
Date: 2011-03-18 03:39:07 UTC
From: AA0ZZ
Topic: 5 Message: 6

Hi Mikey,
The Si570 daughtercard will work fine in any of the PIC-EL board versions. That part of the circuit did not change.
Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "wb8icn" <wb8icn@...> wrote:
>
> I bought the first version of the PIC-EL and really like. The question is will it work with the PPLL-VFO. I read that is does work with version three.
>
> ...Mikey, WB8ICN
>

7. Re: Use with the PIC-EL, version 1

Yahoo group: PPLL-VFO
Date: 2011-03-18 14:13:39 UTC
From: wb8icn
Topic: 5 Message: 7

Thanks Craig!!!
That is what I wanted to hear!!!

...Mikey

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mikey,
> The Si570 daughtercard will work fine in any of the PIC-EL board versions. That part of the circuit did not change.
> Best Regards,
> -Craig, AA0ZZ
>
>
> --- In PPLL-VFO@yahoogroups.com, "wb8icn" <wb8icn@> wrote:
> >
> > I bought the first version of the PIC-EL and really like. The question is will it work with the PPLL-VFO. I read that is does work with version three.
> >
> > ...Mikey, WB8ICN
> >
>

8. Question on Daughtercard

Yahoo group: PPLL-VFO
Date: 2011-03-19 05:00:54 UTC
From: longjohn119
Topic: 8 Message: 8

How compatible/adaptable would this be to one of the common USB Pic contollers like the Softrocks are using?

Basically I have an SDR with a 9951 VFO which works great but is only fully supported by PowerSDR-IQ and none of the others including new versions of PowerSDR-IQ. I'd like to upgrade to one of the Si570 based VFO that is supported by the latest versions of PowerSDR as well as WinRad. Finding the Si570 in single quantities is a problem and I don't need a full SDR kit which is about the only way to get one. I assume they all pretty much program the same and it's just a matter of hooking control/data line to the controller of my choice.

It's not that important that I want to put spend 200 bucks but $41 I can do no problem, I probably have the rest on hand already. I'd just as soon get a kit from Bill as anyone else anyway

JR

9. Re: [PPLL-VFO] Question on Daughtercard

Yahoo group: PPLL-VFO
Date: 2011-03-19 13:28:09 UTC
From: Craig Johnson, AA0ZZ
Topic: 8 Message: 9
Attachments: 2 described; binary payloads are missing from this source WARC

Hi JR,

In a nutshell, they are completely different animals. The software that resides in the PIC in my
control board (or PIC-EL board) and which drives the daughtercard is designed to be stand-alone.
There is no built-n USB controller in the 16F88 PIC and there is no software inside that will talk to
an app over the USB anyway. One of my beta testers (Mert, W0UFO) has interfaced his control board to a Softrock and then to a PC for audio processing and this works fine. My basic desire
is to have an SDR radio of sorts that does not have to be tethered to a PC. This means the user
interface has to be in the PIC and, most significantly, all the complicated Si570 parameter calculations need to be done in the PIC instead of using the horsepower of a PC. I also want
stand-alone audio processing of the I and Q audio outputs.

This will all become more clear with the publication of my QEX article. It has been accepted and
the ARRL editors are working on it but no publication date is set yet. In the mean time, I have sent
you a schematic of Rick's MicroR2 audio section and LNA being interfaced by my Si570 board and
a "Tayloe" commutative mixer. I am currently building this. Another beta tester (W6JR) has interfaced
his control board to his R2Pro for audio processing and it works fine. I have also attached a
schematic of how it can work in a "SoftRock" configuration.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "longjohn119" <russell_john@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Saturday, March 19, 2011 12:00 AM
Subject: [PPLL-VFO] Question on Daughtercard

> How compatible/adaptable would this be to one of the common USB Pic contollers like the Softrocks are using?
>
> Basically I have an SDR with a 9951 VFO which works great but is only fully supported by PowerSDR-IQ and none of the others
> including new versions of PowerSDR-IQ. I'd like to upgrade to one of the Si570 based VFO

that is supported by the latest versions
> of PowerSDR as well as WinRad. Finding the Si570 in single quantities is a problem and I don't need a full SDR kit which is about
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> controller of my choice.
>
> It's not that important that I want to put spend 200 bucks but $41 I can do no problem, I probably have the rest on hand already.
> I'd just as soon get a kit from Bill as anyone else anyway
>
> JR
>
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> Yahoo! Groups Links
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10. Re: Question on Daughtercard - more

Yahoo group: PPLL-VFO
Date: 2011-03-19 16:01:38 UTC
From: AA0ZZ
Topic: 8 Message: 10

Folks,

I have posted some example usage schematics and block diagrams in the FILES section. When the QEX article comes out I will be able to post it on my web site also. It describes in detail how the software works.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi JR,
>
> In a nutshell, they are completely different animals. The software that resides in the PIC in my
> control board (or PIC-EL board) and which drives the daughtercard is designed to be stand-alone.
> There is no built-n USB controller in the 16F88 PIC and there is no software inside that will talk to
> an app over the USB anyway. One of my beta testers (Mert, W0UFO) has interfaced his control
> board to a Softrock and then to a PC for audio processing and this works fine. My basic desire
> is to have an SDR radio of sorts that does not have to be tethered to a PC. This means the user
> interface has to be in the PIC and, most significantly, all the complicated Si570 parameter
> calculations need to be done in the PIC instead of using the horsepower of a PC. I also want
> stand-alone audio processing of the I and Q audio outputs.
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> This will all become more clear with the publication of my QEX article. It has been accepted and
> the ARRL editors are working on it but no publication date is set yet. In the mean time, I have sent
> you a schematic of Rick's MicroR2 audio section and LNA being interfaced by my Si570 board and
> a "Tayloe" commutative mixer. I am currently building this. Another beta tester (W6JR) has interfaced
> his control board to his R2Pro for audio processing and it works fine. I have also attached a
> schematic of how it can work in a "SoftRock" configuration.
>
> Best Regards,
> -Craig, AA0ZZ
>

>
> ----- Original Message -----
> From: "longjohn119" <russell_john@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Saturday, March 19, 2011 12:00 AM
> Subject: [PPLL-VFO] Question on Daughtercard
>
>
> > How compatible/adaptable would this be to one of the common USB Pic contollers like the Softrocks are using?
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> > Basically I have an SDR with a 9951 VFO which works great but is only fully supported by PowerSDR-IQ and none of the others
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> > It's not that important that I want to put spend 200 bucks but $41 I can do no problem, I probably have the rest on hand already.
> > I'd just as soon get a kit from Bill as anyone else anyway
> >
> > JR
> >
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> > ------------------------------------
> >
> > Yahoo! Groups Links
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11. It Works,,, UP to About

Yahoo group: PPLL-VFO
Date: 2011-03-27 14:57:04 UTC
From: dipoley
Topic: 11 Message: 11

I have the Daughtercard Control Board combo,,, It came up Ok,,, I did the calibration,, calibration complete OK,,, The readout hangs up in the 105 to 110 MHz range,, The frequency is random...

The disply shows the second line on power up Ok V 7.5 etc.

When it changes to frequency mode only the first line is displayed.

The voltages where OK as described in the manual.

Thanks,, info from

Mike

12. Re: It Works,,, UP to About - The Solution

Yahoo group: PPLL-VFO
Date: 2011-03-27 19:45:40 UTC
From: AA0ZZ
Topic: 11 Message: 12

Hi Mike,

First of all, congratulatons on getting your Si570 project up and running. Your report is the first that I've seen.

The problem that you reported is something that we also discovered in the last week or so. When changing the frequency in the control board, it sometimes hangs when the frequency reaches somewhere around 102 to 105 MHz. This problem does not show up when the daughtercard is in the PIC-EL board.

We are still diagnosing the exact reason for the hang but, fortunately, there is an easy fix. All you need to to is purt some sort of load on the control board RF port. A 50-ohm dummy load is ideal but you could tack a 51 ohm resistor from the center (RF) connection to ground. Other load values may work as well.

We decided that this should not be a show-stopper that needs an immediate fix since, in real applications, the control board's RF output will be fed into follow-on circuitry such as a receiver mixer and it is easy to make it work in test situations.

We are continuing to investigate the details. If someone has ideas about the exact cause, please post them here.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "dipoley" <w2fndssb@...> wrote:
>
> I have the Daughtercard Control Board combo,,, It came up Ok,,, I did the calibration,, calibration complete OK,,, The readout hangs up in the 105 to 110 MHz range,, The frequency is random...
>
> The disply shows the second line on power up Ok V 7.5 etc.
>
> When it changes to frequency mode only the first line is displayed.
>
> The voltages where OK as described in the manual.
>
> Thanks,, info from
>
> Mike
>

13. Re: It Works,,, UP to About - The Solution

Yahoo group: PPLL-VFO
Date: 2011-03-27 20:20:00 UTC
From: dipoley
Topic: 11 Message: 13

Thanks for the input,,, The no load issue did cross my mind but I did not try it.... I swapped the encoder with a optical one that I have on an IQ vfo,, no difference,, I had to stop work on the VFO to go to income tax land,,,I will get back to the VFO this evening...

Thanks again
Mike

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mike,
>
> First of all, congratulatons on getting your Si570 project up and running. Your report is the first that I've seen.
>
> The problem that you reported is something that we also discovered in the last week or so. When changing the frequency in the control board, it sometimes hangs when the frequency reaches somewhere around 102 to 105 MHz. This problem does not show up when the daughtercard is in the PIC-EL board.
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> -Craig, AA0ZZ
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> > The voltages where OK as described in the manual.
> >
> > Thanks,, info from
> >
> > Mike
> >
>

14. Re: It Works,,, UP to About - The Solution

Yahoo group: PPLL-VFO
Date: 2011-03-28 13:49:06 UTC
From: dipoley
Topic: 11 Message: 14

I glued a resistor 51 ohm resistor to the output pads and all is good.
The full range from 10 to 157 is OK...
Now to dig out my old softrock 40's,,,
Thanks
Mike W2FND

--- In PPLL-VFO@yahoogroups.com, "dipoley" <w2fndssb@...> wrote:
>
> Thanks for the input,,, The no load issue did cross my mind but I did not try it.... I swapped the encoder with a optical one that I have on an IQ vfo,, no difference,, I had to stop work on the VFO to go to income tax land,,,I will get back to the VFO this evening...
>
> Thanks again
> Mike
>
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >
> > Hi Mike,
> >
> > First of all, congratulatons on getting your Si570 project up and running. Your report is the first that I've seen.
> >
> > The problem that you reported is something that we also discovered in the last week or so. When changing the frequency in the control board, it sometimes hangs when the frequency reaches somewhere around 102 to 105 MHz. This problem does not show up when the daughtercard is in the PIC-EL board.
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> > We are still diagnosing the exact reason for the hang but, fortunately, there is an easy fix. All you need to to is purt some sort of load on the control board RF port. A 50-ohm dummy load is ideal but you could tack a 51 ohm resistor from the center (RF) connection to ground. Other load values may work as well.
> >
> > We decided that this should not be a show-stopper that needs an immediate fix since, in real applications, the control board's RF output will be fed into follow-on circuitry such as a receiver mixer and it is easy to make it work in test situations.
> >
> > We are continuing to investigate the details. If someone has ideas about the exact cause, please post them here.
> >
> > Best Regards,
> > -Craig, AA0ZZ
> >
> >
> > --- In PPLL-VFO@yahoogroups.com, "dipoley" <w2fndssb@> wrote:

> > >
> > > I have the Daughtercard Control Board combo,,, It came up Ok,,, I did the calibration,, calibration complete OK,,, The readout hangs up in the 105 to 110 MHz range,, The frequency is random...
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> > > The disply shows the second line on power up Ok V 7.5 etc.
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> > > When it changes to frequency mode only the first line is displayed.
> > >
> > > The voltages where OK as described in the manual.
> > >
> > > Thanks,, info from
> > >
> > > Mike
> > >
> >
>

15. Re: It Works,,, UP to About - The Solution

Yahoo group: PPLL-VFO
Date: 2011-03-28 17:26:18 UTC
From: AA0ZZ
Topic: 11 Message: 15

Mike,
Thanks for the report; I'm glad to hear it works.
I assume the "glue" you used was solder. :-)
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "dipoley" <w2fndssb@...> wrote:
>
> I glued a resistor 51 ohm resistor to the output pads and all is good.
> The full range from 10 to 157 is OK...
> Now to dig out my old softrock 40's,,,
> Thanks
> Mike W2FND
>
>
> --- In PPLL-VFO@yahoogroups.com, "dipoley" <w2fndssb@> wrote:
> >
> > Thanks for the input,,, The no load issue did cross my mind but I did not try it.... I swapped the encoder with a optical one that I have on an IQ vfo,, no difference,, I had to stop work on the VFO to go to income tax land,,,I will get back to the VFO this evening...
> >
> > Thanks again
> > Mike
> >
> >
> > --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> > >
> > > Hi Mike,
> > >
> > > First of all, congratulatons on getting your Si570 project up and running. Your report is the first that I've seen.
> > >
> > > The problem that you reported is something that we also discovered in the last week or so. When changing the frequency in the control board, it sometimes hangs when the frequency reaches somewhere around 102 to 105 MHz. This problem does not show up when the daughtercard is in the PIC-EL board.
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> > > We are still diagnosing the exact reason for the hang but, fortunately, there is an easy fix. All you need to to is purt some sort of load on the control board RF port. A 50-ohm dummy load is ideal but you could tack a 51 ohm resistor from the center (RF) connection to ground. Other load values may work as well.
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> > > We are continuing to investigate the details. If someone has ideas about the exact cause, please post them here.
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> > > Best Regards,
> > > -Craig, AA0ZZ
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> > >
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> > > > The voltages where OK as described in the manual.
> > > >
> > > > Thanks,, info from
> > > >
> > > > Mike
> > > >
> > >
> >
>

16. NG0R - daughter card completed

Yahoo group: PPLL-VFO
Date: 2011-04-04 00:59:43 UTC
From: John Hoaglun
Topic: 16 Message: 16

I completed & tested the daughter card today. I posted some details and pictures on my blog at: http://www.hoaglun.com/blog/

I hope to build another daughter card + control board as time permits over the next few days.

I really enjoyed the project. The instructions are pretty simple and every came up and worked as expected. It was fun to plug into the test gear and poke around for a little while tonight.

It was fun to see Craig's project from prototype (last spring) to complete kit (this spring.)

73
--
John Hoaglun
NG0R - EN25
http://www.hoaglun.com

17. Re: NG0R - daughter card completed

Yahoo group: PPLL-VFO
Date: 2011-04-05 16:27:29 UTC
From: AA0ZZ
Topic: 16 Message: 17

Hi John,

--- In PPLL-VFO@yahoogroups.com, John Hoaglun <john@...> wrote:
>
> I completed & tested the daughter card today. I posted some details and
> pictures on my blog at: http://www.hoaglun.com/blog/
>
> I hope to build another daughter card + control board as time permits
> over the next few days.
>
> I really enjoyed the project. The instructions are pretty simple and
> every came up and worked as expected. It was fun to plug into the test
> gear and poke around for a little while tonight.
>
> It was fun to see Craig's project from prototype (last spring) to
> complete kit (this spring.)
>
> 73
> --
> John Hoaglun
> NG0R - EN25
> http://www.hoaglun.com
>
Congratulations on getting it running. Nice blog! Thanks.
Best Regards,
-Craig, AA0ZZ

18. IF offset

Yahoo group: PPLL-VFO
Date: 2011-05-22 08:40:26 UTC
From: gm4toe
Topic: 18 Message: 18

Has anybody modified the software to include an IF offset in the display before I try to do the job myself?

Barry GM4TOE

19. Re: IF offset

Yahoo group: PPLL-VFO
Date: 2011-05-23 00:49:46 UTC
From: aa0zz
Topic: 18 Message: 19

Hi Barry,

--- In PPLL-VFO@yahoogroups.com, "gm4toe" <barryhorning@...> wrote:
>
> Has anybody modified the software to include an IF offset in the display before I try to do the job myself?
>
> Barry GM4TOE
>
I haven't heard of anyone else doing it yet but it's a good project.
Let me know if you have questions.

Best Regards,
-Craig, AA0ZZ

20. New version of PEgen570 code available

Yahoo group: PPLL-VFO
Date: 2011-05-25 02:30:39 UTC
From: AA0ZZ
Topic: 20 Message: 20

Hi,

A few days ago, Bill Kelsey and I discovered a bug in the PEgen570 code. Nobody else has reported it but I want to make everyone aware of it so you can get your PIC updated if you want to. The bug is in the "divide by 4" code - the code that displays a frequency that is the actual frequency divided by 4. Also a bit of "frequency creeping" when enabling this option.

I have a new version of the code (version 7.6) in the FILES section of this group and on my web page, www.cbjohn.com/aa0zz . If you want to download it and use your programmer (PIC-EL or similar) to update it, that is your quickest and easiest option. If you want us to update it, you can return your PIC to Bill Kelsey at Kanga and he will update it and return it.

By the way, I have also added one minor feature to this new version. I now save the menu selection (1x / 2x / 4x) and (U / L / + / -) in EEPROM so that it is remembered acrooss power-ups.

Best Regards,
-Craig, AA0ZZ

21. IF Shift routine

Yahoo group: PPLL-VFO
Date: 2011-06-28 17:11:26 UTC
From: gm4toe
Topic: 21 Message: 21

I have uploaded to the Files section a little piece of code to add to the firmware for the PIC which will shift the display by an amount equal to the IF in a superhet. This is inserted after the label "bin2BCD" and simply adds four bytes to the Rfreq_* bytes used for displaying frequency on the display.

It would have been simpler to add four variables into the body of the code but I didn't want to mess around with the major items (because I am not certain I fully understand what is going on!). The code takes the bytes for the IF (in this case 10.7MHz) and adds them sequentially starting at the LSB and takes into account the CARRY when the byte addition overflows. Because the addition could overflow over more than one byte (the next byte could be 0hFF) there is a slight complexity as the command "incf" does not affect the CARRY bit in the STATUS register so the addition is a bit convoluted. No real problems it just adds a few microseconds to the calculation for the display.

I have not modified it for subtract but it would not be too difficult to modify if the IF were to be subtracted from the VFO frequency.

Any comments (or improvements) welcomed.

Now to try and work out what else is happening as I would like to make some other modifications to suit my particular (some may say - strange)requirements.

73

Barry GM4TOE

22. Re: IF Shift routine

Yahoo group: PPLL-VFO
Date: 2011-06-28 17:18:31 UTC
From: gm4toe
Topic: 21 Message: 22

Sorry, I should add - don't use this if you are using the divide by 2 or divide by 4 facilities, you will get very strange results!!

73

Barry GM4TOE

--- In PPLL-VFO@yahoogroups.com, "gm4toe" <barryhorning@...> wrote:
>
> I have uploaded to the Files section a little piece of code to add to the firmware for the PIC which will shift the display by an amount equal to the IF in a superhet. This is inserted after the label "bin2BCD" and simply adds four bytes to the Rfreq_* bytes used for displaying frequency on the display.
>
> It would have been simpler to add four variables into the body of the code but I didn't want to mess around with the major items (because I am not certain I fully understand what is going on!). The code takes the bytes for the IF (in this case 10.7MHz) and adds them sequentially starting at the LSB and takes into account the CARRY when the byte addition overflows. Because the addition could overflow over more than one byte (the next byte could be 0hFF) there is a slight complexity as the command "incf" does not affect the CARRY bit in the STATUS register so the addition is a bit convoluted. No real problems it just adds a few microseconds to the calculation for the display.
>
> I have not modified it for subtract but it would not be too difficult to modify if the IF were to be subtracted from the VFO frequency.
>
> Any comments (or improvements) welcomed.
>
> Now to try and work out what else is happening as I would like to make some other modifications to suit my particular (some may say - strange)requirements.
>
> 73
>
> Barry GM4TOE
>

23. Daughter board with PIC EL

Yahoo group: PPLL-VFO
Date: 2011-07-06 21:14:22 UTC
From: vpt7388
Topic: 23 Message: 23

In order to use the earlier versions of PIC EL with the SI570 daughter board, you will need to eliminate the xtal and associated capacitors and insert two 10k resistors to supply, as pull ups instead .

However, I am just getting menu 1,2,3, and 4 and sometimes menu 3 skips !
I am unable to access the menu.
The manual does not say much as to how maipulate the menu and what does menu 1,2,3,4, stand for.
The frequency of the SI570 varies ok, but that is all I could get !!

24. Re: [PPLL-VFO] Daughter board with PIC EL

Yahoo group: PPLL-VFO
Date: 2011-07-06 23:57:39 UTC
From: Craig Johnson, AA0ZZ
Topic: 23 Message: 24

Hi,

The early PIC-EL boards do not have to be modified to remove the crystal and associated capacitors but they do have to
be modified as you say if you want to use those pins as I/O pins. This hardware is exactly the same in the PIC-EL III.

When using the 16F88 PIC in the PIC-EL and running the PEgen570 application, the configuration lines tell the PIC to
ignore the crystal and to use the internal 8 MHz oscillator instead. The two pins for the crystal cannot be used as I/O pins
when in the PIC-EL unless traces are cut and pull-ups added, as you suggest, so some of the functionality of the PEgen570
application cannot be used. When the daughtercard is used in the Control Board the "crystal pins" have the pull-ups and
thus can be used for input signals.

Sorry about the confusion with the menu. The "1,2,3,4" you are asking about is really only 1, 2, and 4 - always. Three is never
displayed. This functionality is used to select the "divide-by-X" mechanism in which the Si570 frequency is divided by the
factor (X) and the resulting frequency is displayed on the LCD. The divide-by-four is often used when folks use the
two flip-flops for generating two quadrature clock signals for use in a QSD/QSE ("Tayloe") mixer. Some mixer schemes
use divide-by-two so that is also offered. If you want the LCD to display the frequency that the Si570 is generating you
leave it as "1".

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "vpt7388" <vpt7388@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Wednesday, July 06, 2011 4:14 PM
Subject: [PPLL-VFO] Daughter board with PIC EL

> In order to use the earlier versions of PIC EL with the SI570 daughter board, you will need to eliminate the xtal and associated
> capacitors and insert two 10k resistors to supply, as pull ups instead .
>
> However, I am just getting menu 1,2,3, and 4 and sometimes menu 3 skips !
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> The frequency of the SI570 varies ok, but that is all I could get !!
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
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>

25. Re: [PPLL-VFO] Daughter board with PIC EL

Yahoo group: PPLL-VFO
Date: 2011-07-07 07:25:12 UTC
From: P X
Topic: 23 Message: 25

Thanks Craig.
However, must say, that when compared to other AVR based similar kits, the AVR has more functions and options in its menu, like lots of memory space, multiplier , divisor, offset, tuning rate, but they suffer from mush, as you tune the encoder. However, the manual is much more comprehensive, when it comes to ser interface.

From: "Craig Johnson, AA0ZZ" <aa0zz@...>
To: PPLL-VFO@yahoogroups.com
Sent: Thursday, July 7, 2011 1:57 AM
Subject: Re: [PPLL-VFO] Daughter board with PIC EL

Hi,

The early PIC-EL boards do not have to be modified to remove the crystal and associated capacitors but they do have to
be modified as you say if you want to use those pins as I/O pins. This hardware is exactly the same in the PIC-EL III.

When using the 16F88 PIC in the PIC-EL and running the PEgen570 application, the configuration lines tell the PIC to
ignore the crystal and to use the internal 8 MHz oscillator instead. The two pins for the crystal cannot be used as I/O pins
when in the PIC-EL unless traces are cut and pull-ups added, as you suggest, so some of the functionality of the PEgen570
application cannot be used. When the daughtercard is used in the Control Board the "crystal pins" have the pull-ups and
thus can be used for input signals.

Sorry about the confusion with the menu. The "1,2,3,4" you are asking about is really only 1, 2, and 4 - always. Three is never
displayed. This functionality is used to select the "divide-by-X" mechanism in which the Si570 frequency is divided by the
factor (X) and the resulting frequency is displayed on the LCD. The divide-by-four is often used when folks use the
two flip-flops for generating two quadrature clock signals for use in a QSD/QSE ("Tayloe") mixer. Some mixer schemes
use divide-by-two so that is also offered. If you want the LCD to display the frequency that the Si570 is generating you
leave it as "1".

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "vpt7388" <vpt7388@...>
To: <PPLL-VFO@yahoogroups.com>

Sent: Wednesday, July 06, 2011 4:14 PM
Subject: [PPLL-VFO] Daughter board with PIC EL

> In order to use the earlier versions of PIC EL with the SI570 daughter board, you will need to eliminate the xtal and associated
> capacitors and insert two 10k resistors to supply, as pull ups instead .
>
> However, I am just getting menu 1,2,3, and 4 and sometimes menu 3 skips !
> I am unable to access the menu.
> The manual does not say much as to how maipulate the menu and what does menu 1,2,3,4, stand for.
> The frequency of the SI570 varies ok, but that is all I could get !!
>
>
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> Yahoo! Groups Links
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26. Re: Daughter board with PIC EL

Yahoo group: PPLL-VFO
Date: 2011-07-07 15:38:45 UTC
From: AA0ZZ
Topic: 23 Message: 26

Hi,

I will fix up the manual to clarify the menu operation. In my first versions of the software the divide-by-x option was selected via a compile option (change a #define statement in source code) so new code had to be assembled and loaded into the PIC to change it. When I changed the code to make the divide-by-x option selectable as a menu option, I changed the manual but did not describe it clearly enough. I will fix it.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
> Thanks Craig.
> However, must say, that when compared to other AVR basedÂ similar kits, the AVR hasÂ more functions and options in its menu, like lots of memory space, multiplier , divisor, offset, tuning rate, but they suffer from mush, as you tune the encoder. However, the manual is much more comprehensive, when it comes to ser interface.
>
>
> _____
> From: "Craig Johnson, AA0ZZ" <aa0zz@...>
> To: PPLL-VFO@yahoogroups.com
> Sent: Thursday, July 7, 2011 1:57 AM
> Subject: Re: [PPLL-VFO] Daughter board with PIC EL
>
>
> Â
> Hi,
>
> The early PIC-EL boards do not have to be modified to remove the crystal and associated capacitors but they do have to
> be modified as you say if you want to use those pins as I/O pins. This hardware is exactly the same in the PIC-EL III.
>
> When using the 16F88 PIC in the PIC-EL and running the PEgen570 application, the configuration lines tell the PIC to
> ignore the crystal and to use the internal 8 MHz oscillator instead. The two pins for the crystal cannot be used as I/O pins
> when in the PIC-EL unless traces are cut and pull-ups added, as you suggest, so some of the functionality of the PEgen570
> application cannot be used. When the daughtercard is used in the Control Board the "crystal pins" have the pull-ups and
> thus can be used for input signals.
>
> Sorry about the confusion with the menu. The "1,2,3,4" you are asking about is really

only 1, 2, and 4 - always. Three is never
> displayed. This functionality is used to select the "divide-by-X" mechanism in which the Si570 frequency is divided by the
> factor (X) and the resulting frequency is displayed on the LCD. The divide-by-four is often used when folks use the
> two flip-flops for generating two quadrature clock signals for use in a QSD/QSE ("Tayloe") mixer. Some mixer schemes
> use divide-by-two so that is also offered. If you want the LCD to display the frequency that the Si570 is generating you
> leave it as "1".
>
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "vpt7388" <vpt7388@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Wednesday, July 06, 2011 4:14 PM
> Subject: [PPLL-VFO] Daughter board with PIC EL
>
> > In order to use the earlier versions of PIC EL with the SI570 daughter board, you will need to eliminate the xtal and associated
> > capacitors and insert two 10k resistors to supply, as pull ups instead .
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> > The manual does not say much as to how maipulate the menu and what does menu 1,2,3,4, stand for.
> > The frequency of the SI570 varies ok, but that is all I could get !!
> >
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> > ------------------------------------
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> > Yahoo! Groups Links
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27. Re: PEgen570 Menu operation

Yahoo group: PPLL-VFO
Date: 2011-07-08 02:04:08 UTC
From: Craig Johnson, AA0ZZ
Topic: 27 Message: 27

Hi folks,
Here's a follow-up to my previous message re clarifying the Menu operation in the manual. Here's the relevant text. I will have the new version of the manual in the FILES section and on my web page shortly.
========
1.1 Menu
A simple menu is used for changing 3 items in the operation.

1) Sideband selection

2) Frequency division for LCD display

3) FSK enable (if FSK is enabled via compile option in source code)

The menu is activated by holding Pushbutton 4 while pushing Pushbutton 3 and then releasing them both. The current mode is shown in
character position 1 of line 1 of the LCD. Now the user can update the current selection of each of the three items. Tapping
Pushbutton 3 allows the user to cycle through the available options for the current item. Tapping Pushbutton 4 leaves the current
item at its last value and advances to the next item in the menu. After the last item has been selected, pressing Pushbutton 4
exits the menu.

1.1.1 Sideband Selection
The first menu item that may be selected in the menu is the sideband selection. The user may select one of four sideband modes,
USB, LSB, CW+ or CW- .

An external latching relay is engaged or disengaged as the sideband is changed in the menu. PIC output ports RA6 and RA7 attach to
HDR5 and HDR6 (pins 15 and 16) respectively. As the sideband is changed in the menu, either RA6 or RA7 is driven high with an 8 mS
pulse (with the opposite side being held low) to engage or disengage the external latching relay. The recommended latching relay
(TQ2-L-5V - DigiKey part 255-1004-5-ND) requires 14 mA at 5v for 3 mS plus contact bounce time. The latching relay is intended to
enable the proper I and Q phases of the transmitter and/or receiver to set the proper sideband.

1.1.2 CW Sidetone During Receive
If the mode is CW+ or CW- , Header HDR7, attached to PIC input port PB7, is monitored by the software to determine whether or not to
shift the frequency by the sidetone amount. HDR7 is expected to be set to a low state by external Transmit/Receive circuitry
during Receive operations and to a high state during Transmit operations. The software continually monitors the signal at HDR7 and,

when is detected to be low while in CW- mode, shifts the frequency down by 600 Hz from the nominal, displayed frequency. If the
mode is CW+ and HDR7 is LOW (Receive), the frequency is shifted up by 600 Hz from the nominal, displayed frequency. In either case,
whenever HDR7 is detected to be HIGH, indicating Transmit operation, the frequency will be set back to the nominal frequency that is
displayed on the LCD.

How fast does it switch? The software looks at the signal on HDR7 often enough to detect and change the frequency within 1.6 mS of
HDR7 changing state. That's fast enough for QSK.

1.1.3 Frequency Division for LCD Display
The PEgen570 application can be configured to display the current Si570 generated frequency or it can be configured to display the
Si570 frequency divided by two or four. The divide-by-four option is useful when the signal generator is being used as a signal
source for a QSD/QSE ("Tayloe") mixer. The circuitry for these mixers usually divides the input frequency by four so this software
option allows the LCD to display the mixer's operating frequency.

Tapping PB3 while in this portion of the menu allows the divide-by-x factor to be changed. When the correct factor is selected,
press PB4 to advance to the next menu item selection.

1.1.4 FSK Frequency Shift
This menu item is only available and displayed only if the FSK option is enabled via a #DEFINE statement in the source code. The
default software does not have FSK enabled.

Tapping PB3 while in this portion of the menu allows the FSK option to be enabled or disabled. When the correct factor is selected,
press PB4 to advance to the next menu item selection.

If FSK is enabled, the FSK shift size will be used, even if CW+ or CW- is also selected in the menu. FSK takes precedence.

When FSK is active, Header HDR7, attached to PIC input port PB7, is monitored by the software to determine whether or not to shift
the frequency by the FSK shift size. The frequency is set to the displayed frequency when the signal on HDR7 is HIGH (the MARK
frequency) and is shifted down by 170 Hz when the signal on HDR7 is LOW (the SPACE frequency).

The software looks at the signal on HDR7 often enough to detect and change the frequency within 1.6 mS of HDR7 changing state.

1.2 LCD Display
The first line of the LCD displays the current frequency. The second line is for debug purposes and shows the hex digits for the 6
Si570 register parameter (SiReg7 through SiReg12) starting at LCD position 1. The current band number is displayed in positions 15

and 16 of line 2.

As explained in the Menu section regarding the frequency division selection option, the PEgen570 application can be configured to
display the current Si570 frequency or it can be configured to display the Si570 frequency divided by two or four. The
divide-by-four option is useful when the signal generator is being used as a signal source for a QSD/QSE ("Tayloe") mixer. The
circuitry for these mixers usually divides the input frequency by four so this software option allows the LCD to display the mixer's
operating frequency.

==========

Hope this helps.

Best Regards,
-Craig, AA0ZZ

28. Updated user manuals in FILES section

Yahoo group: PPLL-VFO
Date: 2011-07-08 03:10:50 UTC
From: AA0ZZ
Topic: 28 Message: 28

Hi,
I have uploaded new versions of the Daughtercard and Control Board user manuals to the FILES section. Only change was the update of the MENU section.

I have also uploaded my Si570 article to the FILES section. This is very similar to my QEX article (July/August issue) but is in PDF format. This article gives many details regarding how the Si570 works, how the two boards work, and how the PEgen570 application works. Also several application schematics.

All files have also been updated on my web page, www.cbjohn.com/aa0zz .

Best Regards,
-Craig, AA0ZZ

29. Signal Generator

Yahoo group: PPLL-VFO
Date: 2011-07-09 05:09:16 UTC
From: ag4qc
Topic: 29 Message: 29

I'm thinking this Si570 project would make a nice signal generator. But it's output being a square wave would be an issue. So I was think of making a few filters to suppress the harmonics. Also I would probably need some sort of variable level control. None of this is rocket science, but before I dive into this, I was wondering if anyone had already built such an animal? I was thinking of maybe switching band pass filters as an adjunct to the pic setting the frequency.. Ah, never a dull moment.

Joe Loucka AG4QC

30. Re: [PPLL-VFO] Signal Generator

Yahoo group: PPLL-VFO
Date: 2011-07-09 07:27:14 UTC
From: M5FRA - Colin
Topic: 29 Message: 30

Joe, there are other versions of the Si570 that give a sine wave output.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "ag4qc" <ag4qc@...>
To: PPLL-VFO@yahoogroups.com
Sent: 09/07/2011 06:09:16
Subject: [PPLL-VFO] Signal Generator
>I'm thinking this Si570 project would make a nice signal generator. But it's output being a square wave would be an issue. So I was think of making a few filters to suppress the harmonics. Also I would probably need some sort of variable level control. None of this is rocket science, but before I dive into this, I was wondering if anyone had already built such an animal? I was thinking of maybe switching band pass filters as an adjunct to the pic setting the frequency.. Ah, never a dull moment.
>
>Joe Loucka AG4QC
>
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>------------------------------------
>
>Yahoo! Groups Links
>
>http://groups.yahoo.com/group/PPLL-VFO/
>
>http://groups.yahoo.com/group/PPLL-VFO/join
> (Yahoo! ID required)
>
>
>http://docs.yahoo.com/info/terms/
>
>
>

31. New to the list + RIT

Yahoo group: PPLL-VFO
Date: 2011-07-09 07:33:38 UTC
From: M5FRA - Colin
Topic: 31 Message: 31

I am new to the list but not new to the Si570. I have a small stand alone VFO which is the basis of a 80-10m CW TX/RX. I want to use one of the Kanga kits in a small 3/4 band CW TX/RX for portable use but have a couple of questions. The first is how to implement RIT? And using an RX strip similar to the MicroR2 how can I get narrow selectivity other than by using audio filtering? This is not a major probelm as I use SCAF filters on other simple rigs with great success. Having RIT is an issue.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

32. Re: [PPLL-VFO] Signal Generator and RIT

Yahoo group: PPLL-VFO
Date: 2011-07-09 14:16:18 UTC
From: Craig Johnson, AA0ZZ
Topic: 32 Message: 32

Hi Joe and Colin,

I will not say much right now regarding the square-to-sine issue but I think a simple filter could do it. I'm sure others will weigh in with some ideas.

Colin, your question about implementing RIT (Receive Increment Tuning) is interesting. There is an receive offset implemented now - offsetting the frequency by the "sidetone amount" when receiving while both stations have the same transmitting frequency. HDR7 is monitored to allow the PIC to know when it's in XMIT mode and when it's in RCV mode. The "sidetone amount" is currently fixed at 600 Hz but if this value was made to be variable and adjustable then it would be an RIT. It certainly can be done - it's just software. :-) With this hardware implementation and limited number of I/O pins on the PIC we only have two pushbuttons and we would like to have to have a way to quickly activate / deactivate / adjust the RIT. Assuming that this can be figured out, I could see the encoder being used to adjust the "sidetone amount" without changing the transmitter frequency. This will take some careful thought before starting to implement it but it's certainly possible There is plenty of room left in the PIC.

Perhaps we can kick around some implementation ideas here.

Best Regards,
-Craig, AA0ZZ
----- Original Message -----
From: M5FRA - Colin
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 09, 2011 2:33 AM
Subject: [PPLL-VFO] New to the list + RIT

I am new to the list but not new to the Si570. I have a small stand alone VFO which is the basis of a 80-10m CW TX/RX. I want to use one of the Kanga kits in a small 3/4 band CW TX/RX for portable use but have a couple of questions. The first is how to implement RIT? And using an RX strip similar to the MicroR2 how can I get narrow selectivity other than by using audio filtering? This is not a major probelm as I use SCAF filters on other simple rigs with great success. Having RIT is an issue.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

33. Si571 source and reference design for > 160 MHz?

Yahoo group: PPLL-VFO
Date: 2011-07-09 16:16:53 UTC
From: cruizzer77
Topic: 33 Message: 33

Hi

I just joined the list after seeing the article in QEX. Sometimes it's funny, just a few days ago I looked into the Si571 device after I had read about it, and now comes an article about it!

The Si571 device has a control voltage input which means it can be fm-modulated very easily, otherwise it's the same as the Si570.

Does by chance anyone know a source where these devices can be had in the 'A'-version, the one that will make up to 1.4 GHz, or the 'B'-version which will go to 810 MHz? Both of these ranges will be LVDS output instead of CMOS, does someone maybe even have a reference design for these?

73
Martin HB9TZW

34. Re: Signal Generator

Yahoo group: PPLL-VFO
Date: 2011-07-10 00:24:16 UTC
From: kb1gmx
Topic: 29 Message: 34

--- In PPLL-VFO@yahoogroups.com, "ag4qc" <ag4qc@...> wrote:
>
> I'm thinking this Si570 project would make a nice signal generator. But it's output being a square wave would be an issue. So I was think of making a few filters to suppress the harmonics. Also I would probably need some sort of variable level control. None of this is rocket science, but before I dive into this, I was wondering if anyone had already built such an animal? I was thinking of maybe switching band pass filters as an adjunct to the pic setting the frequency.. Ah, never a dull moment.
>
> Joe Loucka AG4QC
>

I took a swipe at this and the solution was simple. Use the SI570 from 80mhz to 160mhz, pass that through a low pass filter then mix the result with a 80mhz crystal osc to get a DC to 79mhz result
that goes to a low pas filter for further clean up. The result is a clean sine wave, 1hz accuracy (for mine) and good stability and repeatability. I did later add some level control of the output
by using a shielded attenuator after a fixed pad. The result is a well shielded signal that can easily be attenuated from -20dbm to
-80dbm without external pads and good enough shielding to hit
-140dbm with accuracy (+-3db) in the HF to 6M range.

The approach seems complicated but only two filters were needed. a commercial DBM (Minicircuits TFM2 1-1000mhz) found at a ham flea
and the attenuator was a handbook step switched affair.

It was easy to shield as the two RF sources (osc and si570) were
working above the range of mixed output. Nothing magical save for watching the levels fed to the mixer and very building block.

Allison

35. Re[2]: [PPLL-VFO] Signal Generator and RIT

Yahoo group: PPLL-VFO
Date: 2011-07-10 08:18:34 UTC
From: M5FRA - Colin
Topic: 32 Message: 35

Craig, thanks for the commenst. I wish I could help with the software but am strictly a hardware person! I am using an Si570 VFO on another yet to be completed rig and the same issue arose. The RX is a superhet with 9mhz IF and my quick fiddle was to put a varicap across the CIO xtal with a pot on the front panel to alter frequency slightly. Not the best solution but essential when working with narrow AF filters.

I have been looking at the R2 design in Experiemental Methods in RF Design and found the passive audio filters. I am sure they work and will include the basic 3khz filter but will stick with my idea of using a SCAF filter for lower bandwidths. I am now thinking of ordering an R2Pro kit to play around with.

So, I can offer moral support and am willing to test out new software. I am sorry I am not a software coder, just a bit too old....

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "Craig Johnson, AA0ZZ" <aa0zz@...>
To: PPLL-VFO@yahoogroups.com
Sent: 09/07/2011 15:16:18
Subject: Re: [PPLL-VFO] Signal Generator and RIT
>□
>
>Hi Joe and Colin,
>
>I will not say much right now regarding the square-to-sine issue but I
>think a simple filter could do it. I'm sure others will weigh in
>with some ideas.
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>Colin, your question about implementing RIT (Receive Increment Tuning)
>is interesting. There is an receive offset implemented now -
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>both stations have the same transmitting frequency. HDR7 is monitored
>to allow the PIC to know when it's in XMIT mode and when it's in RCV
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>value was made to be variable and adjustable then it would be an RIT.
> It certainly can be done - it's just software. :-) With this
>hardware implementation and limited number of I/O pins on the PIC we
>only have two pushbuttons and we would like to have to have a way to
>quickly activate / deactivate / adjust the RIT. Assuming that this
>can be figured out, I could see the encoder being used to adjust the
>"sidetone amount" without changing the transmitter frequency. This

>will take some careful thought before starting to implement it but
>it's certainly possible There is plenty of room left in the PIC.
>
>Perhaps we can kick around some implementation ideas here.
>
>Best Regards,
>-Craig, AA0ZZ
>>----- Original Message -----
>>From:M5FRA - Colin
>>To:PPLL-VFO@yahoogroups.com
>>Sent: Saturday, July 09, 2011 2:33 AM
>>Subject: [PPLL-VFO] New to the list + RIT
>>
>>I am new to the list but not new to the Si570. I have a small stand
>>alone VFO which is the basis of a 80-10m CW TX/RX. I want to use one
>>of the Kanga kits in a small 3/4 band CW TX/RX for portable use but
>>have a couple of questions. The first is how to implement RIT? And
>>using an RX strip similar to the MicroR2 how can I get narrow
>>selectivity other than by using audio filtering? This is not a major
>>probelm as I use SCAF filters on other simple rigs with great
>>success. Having RIT is an issue.
>>
>>Colin - G8FRA/M5FRA
>>
>>http://www.m5fra.org.uk/
>>
>
>
>

36. SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 12:12:24 UTC
From: vpt7388
Topic: 36 Message: 36

The SI570 versions:

CAC is CMOS up to 160Mhz, reported up to 280Mhz, output 3 volts

BBB is LVDS up to 810Mhz, reported up to 910Mhz with 0.7 volts out

BBC is LVDS up to 280Mhz output 0.7 volts

DBA up to 1417Mhz with 1.5 volts CML level

The SI570 is CMOS, up to 210Mhz with FM

The LVDS level can be boosted up by a simple FIN1002 chip, up to over 3 volts.

Many microcontrollers, have the option to control all versions of the SI570 by a built in memory option in the menu to extend the frequency range.

37. Re: SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 18:36:55 UTC
From: AA0ZZ
Topic: 36 Message: 37

Humm... that's interesting.

It wouldn't be very difficult to mount one of the LVDS parts on the daughtcard, run coax from the two output pads on the daughtercard to a FIN1002 (probably off board) and then it would work way up there in the VHF / UHF regions. It would not be hard to update the band tables (4 bytes per band, specifying the lower band limit in MHz) to reach these regions. It's just the total number of bands that would be a little more difficult to handle.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
>
> The SI570 versions:
>
> CAC is CMOS up to 160Mhz, reported up to 280Mhz, output 3 volts
>
> BBB is LVDS up to 810Mhz, reported up to 910Mhz with 0.7 volts out
>
> BBC is LVDS up to 280Mhz output 0.7 volts
>
> DBA up to 1417Mhz with 1.5 volts CML level
>
> The SI570 is CMOS, up to 210Mhz with FM
>
> The LVDS level can be boosted up by a simple FIN1002 chip, up to over 3 volts.
>
> Many microcontrollers, have the option to control all versions of the SI570 by a built in memory option in the menu to extend the frequency range.
>

38. Re: SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 18:44:44 UTC
From: Stephen Farthing
Topic: 36 Message: 38

Guys,

Check out www.sdr-kits.net who sell both 2 synth kits and also sell the various grades of Si570. I am working on an Arduino (thats a microcontroller board) controlled Si570 synth but progress is slow.

73s Steve

--
It is vain to do with more that which can be done with less.

39. Re: [PPLL-VFO] Re: SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 18:57:54 UTC
From: Craig Johnson, AA0ZZ
Topic: 36 Message: 39

The parts are also available directly from Silicon Labs in large or small quantities and then you can specify the start-up frequency that you want.
www.silabs.com I use 10 MHz as the start-up frequency.

-Craig
----- Original Message -----
From: Stephen Farthing
To: PPLL-VFO@yahoogroups.com
Sent: Sunday, July 10, 2011 1:44 PM
Subject: [PPLL-VFO] Re: SI570 versions

Guys,

Check out www.sdr-kits.net who sell both 2 synth kits and also sell the various grades of Si570. I am working on an Arduino (thats a microcontroller board) controlled Si570 synth but progress is slow.

73s Steve

--
It is vain to do with more that which can be done with less.

40. Re: [PPLL-VFO] Re: SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 21:37:57 UTC
From: P X
Topic: 36 Message: 40

The AVR controller versions will work with all versions of the SI570 . I know, because I have four kits all controlled by an AVR controller and you can memorise the various ham band with various options, say, 40m with a times 4 multiplier and another memory with 20m with times 2 multipler memory ! Up to say 100 memoories !!! I must confess that the PIC type of microcontroller has a very limited emeory allocatio0ns as compared to to an avr !!

41. Re: [PPLL-VFO] Re: SI570 versions

Yahoo group: PPLL-VFO
Date: 2011-07-10 21:45:19 UTC
From: P X
Topic: 36 Message: 41

These two kits suppliers have a a very good si570 controlled kits, extending to well above the specified frequency range, but they both suffer from mush or noise, as you tune a dx frequency !!!

http://sdr-kits.net/PAOKLT/PAOKLT.html

http://www.qsl.net/k5bcq/Kits/Kits.html

42. Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-10 21:51:40 UTC
From: vpt7388
Topic: 42 Message: 42

Many si570 kits suffer from one major defect: as you tune the frequency, thay produce lots of artivfacts, like noise, mus and all sorts of annoying noise and it will be impossible to pick up a dx station in the tuning noise. This is never mentioned by the kits suppliers ! Indeed, one supplier claims that the vfo is smooth, but in practice it is not smooth at all, full of of articats as you tune with your encoder !!!!!

I know, becaue I have four kits , all fully funcioning, but all suffer from this tuning artifact !!!!!

43. Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-10 23:25:21 UTC
From: AA0ZZ
Topic: 42 Message: 43

OK, I need to ask. Which kits did you test and what kind of noise did you find? Do you mean the "pop" than can occur on each frequency change if the programmer did not do the update properly? Or other noise?

A "pop" can occur when the Si570 is stopped and then restarted at a new frequency. It does not have to occur, however, and it does not occur in my Si570 kit since I determined the cause and changed the software to prevent it.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
>
> Many si570 kits suffer from one major defect: as you tune the frequency, thay produce lots of artivfacts, like noise, mus and all sorts of annoying noise and it will be impossible to pick up a dx station in the tuning noise. This is never mentioned by the kits suppliers ! Indeed, one supplier claims that the vfo is smooth, but in practice it is not smooth at all, full of of articats as you tune with your encoder !!!!!
>
> I know, becaue I have four kits , all fully funcioning, but all suffer from this tuning artifact !!!!!
>

44. Re: [PPLL-VFO] Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-11 06:06:43 UTC
From: M5FRA - Colin
Topic: 42 Message: 44

Not my experience.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "vpt7388" <vpt7388@...>
To: PPLL-VFO@yahoogroups.com
Sent: 10/07/2011 22:51:40
Subject: [PPLL-VFO] Be careful with SI570 kits !!!!!
>Many si570 kits suffer from one major defect: as you tune the frequency, thay produce lots of artivfacts, like noise, mus and all sorts of annoying noise and it will be impossible to pick up a dx station in the tuning noise. This is never mentioned by the kits suppliers ! Indeed, one supplier claims that the vfo is smooth, but in practice it is not smooth at all, full of of articats as you tune with your encoder !!!!!
>
>I know, becaue I have four kits , all fully funcioning, but all suffer from this tuning artifact !!!!!
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>http://groups.yahoo.com/group/PPLL-VFO/join
> (Yahoo! ID required)
>
>
>http://docs.yahoo.com/info/terms/
>
>
>

45. Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-11 10:18:51 UTC
From: P X
Topic: 42 Message: 45

What I mean is that when the encoder is turned to change frequency , even a few cycles up or down, there is a noise, similar to an rx backround noise. I have not yet tested your kit, but this effect was noticed on other AVR based kits.

46. Re: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-11 10:56:12 UTC
From: M5FRA - Colin
Topic: 42 Message: 46

I have just done some test on MY RX and cannot hear any increase in noise as the VFO is tuned. There is the usual 'plop' which causes the AGC to react but I cannot hear anything else. The RX is sensitive but can have the RF amp turned off. Again no noticeable chamge in background noise when tuning. The RX is a superhet with a 9mhz IF.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "P X" <vpt7388@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 11/07/2011 11:18:51
Subject: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!
>
>
>
>What I mean is that when the encoder is turned to change frequency ,
>even a few cycles up or down, there is a noise, similar to an rx
>backround noise. I have not yet tested your kit, but this effect was
>noticed on other AVR based kits.
>
>
>

47. Re: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-11 11:48:36 UTC
From: Craig Johnson, AA0ZZ
Topic: 42 Message: 47

OK. That's different, and isn't necessarily due to the Si570. This would take some careful analysis with a spectrum analyzer to
determine what's going on.

I just want to make sure we are very careful when we talk about the performance of the Si570 kits.

-Craig
----- Original Message -----
From: P X
To: PPLL-VFO@yahoogroups.com
Sent: Monday, July 11, 2011 5:18 AM
Subject: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!

What I mean is that when the encoder is turned to change frequency , even a few cycles up or down, there is a noise, similar to an rx backround noise. I have not yet tested your kit, but this effect was noticed on other AVR based kits.

48. Daughtercard schematic

Yahoo group: PPLL-VFO
Date: 2011-07-13 00:05:14 UTC
From: AA0ZZ
Topic: 48 Message: 48

Hi Folks,

It was just pointed out to me by Jim Dunlap, WB5ZOR, that I had an error in the Daughtercard schematic. Don't panic - it doesn't affect the operation of the Daughtercard or the Control Board or the software but the Si570 Clock and Data lines that go to the PIC-EL connector pins were reversed and did not agree with the actual traces on the board.

I have updated the Daughtercard schematic, the user manual and my Si570 Article (similar to my QEX article but with figures in-line and in color) in the FILES section and on my web page.

Thanks for finding this pointing it out, Jim.

Best Regards,
-Craig, AA0ZZ

49. microR2 and SI570 interfacing

Yahoo group: PPLL-VFO
Date: 2011-07-13 15:41:30 UTC
From: leroy
Topic: 49 Message: 49

I have a micro R2 and a SI570. Schematics provided show

interfacing with FST3225MX/74AC74 circuitry. I looked

into getting parts to try to home brew something, and

see the surface mount devices. Anyone came up with

a PC board or some home brew method of making this work?

Thanks, Roy AB7CE

50. Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-13 20:31:34 UTC
From: kb1gmx
Topic: 42 Message: 50

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
>
>
> What I mean is that when the encoder is turned to change frequency , even a few cycles up or down, there is a noise, similar to an rx backround noise. I have not yet tested your kit, but this effect was noticed on other AVR based kits.
>

That may not be the SI570 at all. To tune you need to send data to it and that is done via a fast serial bus and the resulting signals can and will have harmonics that can get into the radio. BOard layout and signal routing can be a factor in that.

The other source of noise is the CPU can be in a low power mode between tuning steps and the transition between modes can produce power supply spikes and resulting noise.

Both can be influenced by grounding and packaging approaches used.

I have a few of the K5BCQ SI570 boards and while I've not used it
in a radio I have used it for LO on the bench and I have not heard
tuning noise, But that use had the BCQ board running from separate power and only the RF cable between the radio being operated.

Allison

51. Re: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!

Yahoo group: PPLL-VFO
Date: 2011-07-13 23:21:44 UTC
From: P X
Topic: 42 Message: 51

Allison,

You are right. I have both the K5BCQ and the PA0KLT kits and both suffer from this inconvienience. But , they are not screened or enclosed, just laying bare on my workshop bench. When contacted the author, he said that I could try ground the encoder with a 100 ohms resistor . However this did not work. I have tried various bypass methods , but all failed. The remaining thing to do, is as you say- use a seperate psu, or perhaps, raise the ground connection from the psu to the unit with a common mode choke .

_____
From: kb1gmx <kb1gmx@arrl.net>
To: PPLL-VFO@yahoogroups.com
Sent: Wednesday, July 13, 2011 10:31 PM
Subject: [PPLL-VFO] Re: Be careful with SI570 kits !!!!!

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
>
>
> What I mean is that when the encoder is turned to change frequency , even a few cycles up or down, there is a noise, similar to an rx backround noise. I have not yet tested your kit, but this effect was noticed on other AVR based kits.
>

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Both can be influenced by grounding and packaging approaches used.

I have a few of the K5BCQ SI570 boards and while I've not used it
in a radio I have used it for LO on the bench and I have not heard
tuning noise, But that use had the BCQ board running from separate power and only the RF cable between the radio being operated.

Allison

52. compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-13 23:55:41 UTC
From: vpt7388
Topic: 52 Message: 52

Hi all.
I have found a very interesting article comparing DDS with SI570.

http://www.hanssummers.com/ddssi570.html

53. Re: [PPLL-VFO] compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-14 05:45:37 UTC
From: M5FRA - Colin
Topic: 52 Message: 53

Except that the comparison is wrong on several counts:

1) Versions of the Si570 can offer a sine wave output.
2) The frequency range extends down to 3.45Mhz.
3) It is easy to make adjustments to the internal calibration to set
the frequency accurately, stability is excellent.
4) Yes there is a tuning ‘plop’ but that can be eliminated in software.
5) The interface is not tricky just different.
6) The phase noise from the Si570 is as good as some professional
signal generators.
7) As he says at the end he just likes DDS i.e. this is his personal
opinion. What you use is up to you!

My Si570 8 band TX/RX is almost finished, I will tell more when it is
working and had some basic testing. I know there are many others using
similar PPLL-VFOs so there should be some other empirical evidence
around by now.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "vpt7388" <vpt7388@...>
To: PPLL-VFO@yahoogroups.com
Sent: 14/07/2011 00:55:41
Subject: [PPLL-VFO] compare a DDS with the SI570
>Hi all.
>I have found a very interesting article comparing DDS with SI570.
>
>
>http://www.hanssummers.com/ddssi570.html
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>Yahoo! Groups Links
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>http://groups.yahoo.com/group/PPLL-VFO/
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>http://groups.yahoo.com/group/PPLL-VFO/join
> (Yahoo! ID required)
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>http://docs.yahoo.com/info/terms/
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54. Re[2]: [PPLL-VFO] compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-14 12:22:08 UTC
From: M5FRA - Colin
Topic: 52 Message: 54

OK I should have qualified the sine wave bit! The LVDS output is what
many would called a 'modified sine wave'. I put the VFO output through
the RX BPFs (relay switched) before sending to the TX driver stage. The
O/P looks like a very nice sine wave.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "M5FRA - Colin" <m5fra@...>
To: PPLL-VFO@yahoogroups.com
Sent: 14/07/2011 06:45:37
Subject: Re: [PPLL-VFO] compare a DDS with the SI570
>Except that the comparison is wrong on several counts:
>
>1) Versions of the Si570 can offer a sine wave output.
>2) The frequency range extends down to 3.45Mhz.
>3) It is easy to make adjustments to the internal calibration to set
>the frequency accurately, stability is excellent.
>4) Yes there is a tuning ‘plop’ but that can be eliminated in software.
>5) The interface is not tricky just different.
>6) The phase noise from the Si570 is as good as some professional
>signal generators.
>7) As he says at the end he just likes DDS i.e. this is his personal
>opinion. What you use is up to you!
>
>My Si570 8 band TX/RX is almost finished, I will tell more when it is
>working and had some basic testing. I know there are many others using
>similar PPLL-VFOs so there should be some other empirical evidence
>around by now.
>
>Colin - G8FRA/M5FRA
>
>
>www.m5fra.org.uk
>
>
>------ Original Message ------
>From: "vpt7388" <vpt7388@...>
>To: PPLL-VFO@yahoogroups.com
>Sent: 14/07/2011 00:55:41
>Subject: [PPLL-VFO] compare a DDS with the SI570
>
>>
>>Hi all.

>>I have found a very interesting article comparing DDS with SI570.
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>
>

55. Re: microR2 and SI570 interfacing

Yahoo group: PPLL-VFO
Date: 2011-07-14 12:37:07 UTC
From: AA0ZZ
Topic: 49 Message: 55

Leroy,

The SN74AC74 is available in 14-pin DIP format (Digikey 296-4342-5-ND) so it's pretty easy to dead-bug that one. Just put it in a socket and attach wires to the socket legs.

The FST3253MX (16-SOIC format) is not available from Digikey but is available from Mouser (512-FST3253MX). I mounted the SOIC part in a 16-pin SOIC "surfboard" (Digikey 161CA-ND) which I super-glued to my ground-plane board. Then it was easy to attach wires to the pads. I built it all "Manhattan style" with connection points made from 1/8" hole punches made from a piece of PC board and super-glued to the ground-plane board. I'll try to get a picture of it.

I've posted the pad layout that I used for this RX front-end (power supply, SN74AC74 and QSD with FST3253MX, and LT6231) in the FILES section of this group. The Si570 control board feeds into this section and the quadrature audio outputs are fed into the MicroR2 audio section.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "leroy" <lmarion@...> wrote:
>
> I have a micro R2 and a SI570. Schematics provided show
>
> interfacing with FST3225MX/74AC74 circuitry. I looked
>
> into getting parts to try to home brew something, and
>
> see the surface mount devices. Anyone came up with
>
> a PC board or some home brew method of making this work?
>
> Thanks, Roy AB7CE
>

56. Re: [PPLL-VFO] Re: microR2 and SI570 interfacing

Yahoo group: PPLL-VFO
Date: 2011-07-14 13:45:17 UTC
From: P X
Topic: 49 Message: 56

Components for SDR, QSD and phasing techniques can be bought from:
http://thepartsplace.k5nwa.com/

They have no minimum quantity, excellent prices and shipping is down to earth.

Your idea is very similar to the Softrock Lite II

http://www.wb5rvz.com/sdr/sr_lite_ii/

If you eliminate the xtal controlled oscillator and feed the SI570 instead, you have a stand alone QSD front end, with excellent performance. You may have to fiddle with the output of the SI570, because, theoretically there should be enough level to drive the 74AC74, but in practice ?

enjoy

From: AA0ZZ <aa0zz@...>
To: PPLL-VFO@yahoogroups.com
Sent: Thursday, July 14, 2011 2:37 PM
Subject: [PPLL-VFO] Re: microR2 and SI570 interfacing

Leroy,

The SN74AC74 is available in 14-pin DIP format (Digikey 296-4342-5-ND) so it's pretty easy to dead-bug that one. Just put it in a socket and attach wires to the socket legs.

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I've posted the pad layout that I used for this RX front-end (power supply, SN74AC74 and QSD with FST3253MX, and LT6231) in the FILES section of this group. The Si570 control board feeds into this section and the quadrature audio outputs are fed into the MicroR2 audio section.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "leroy" <lmarion@...> wrote:
>
> I have a micro R2 and a SI570. Schematics provided show
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>

> into getting parts to try to home brew something, and
>
> see the surface mount devices. Anyone came up with
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> a PC board or some home brew method of making this work?
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> Thanks, Roy AB7CE
>

57. Re: microR2 and SI570 interfacing

Yahoo group: PPLL-VFO
Date: 2011-07-14 19:15:58 UTC
From: vpt7388
Topic: 49 Message: 57

Youi can also try this universal SI570 baord which will work with any processor !!

http://home.roadrunner.com/~wa6ufq/universal_vfo_controller.html

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
> Components for SDR, QSD and phasing techniques can be bought from:
> http://thepartsplace.k5nwa.com/
>
> They have no minimum quantity, excellent pricesÂ and shipping is down to earth.
>
> Your idea is very similar to the Softrock Lite II
>
> http://www.wb5rvz.com/sdr/sr_lite_ii/
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> If you eliminate the xtal controlled oscillator and feed the SI570 instead, you have aÂ stand alone QSD front end, with excellent performance. You may have to fiddle with the output of the SI570, because, theoretically there should be enough level to drive the 74AC74, but in practice ?
>
> enjoy
>
>
>
> _____
> From: AA0ZZ <aa0zz@...>
> To: PPLL-VFO@yahoogroups.com
> Sent: Thursday, July 14, 2011 2:37 PM
> Subject: [PPLL-VFO] Re: microR2 and SI570 interfacing
>
>
> Â
> Leroy,
>
> The SN74AC74 is available in 14-pin DIP format (Digikey 296-4342-5-ND) so it's pretty easy to dead-bug that one. Just put it in a socket and attach wires to the socket legs.
>
> The FST3253MX (16-SOIC format) is not available from Digikey but is
> available from Mouser (512-FST3253MX). I mounted the SOIC part in a 16-pin SOIC "surfboard" (Digikey 161CA-ND) which I super-glued to my ground-plane board. Then it was easy to attach wires to the pads. I built it all "Manhattan style" with connection points made from 1/8" hole punches made from a piece of PC board and super-glued to the ground-plane board. I'll try to get a picture of it.
>
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>
> Best Regards,
> -Craig, AA0ZZ
>
> --- In PPLL-VFO@yahoogroups.com, "leroy" <lmarion@> wrote:
> >
> > I have a micro R2 and a SI570. Schematics provided show
> >
> > interfacing with FST3225MX/74AC74 circuitry. I looked
> >
> > into getting parts to try to home brew something, and
> >
> > see the surface mount devices. Anyone came up with
> >
> > a PC board or some home brew method of making this work?
> >
> > Thanks, Roy AB7CE
> >
>

58. Re: [PPLL-VFO] Re: microR2 and SI570 interfacing

Yahoo group: PPLL-VFO
Date: 2011-07-14 08:38:04 UTC
From: Leroy Marion
Topic: 49 Message: 58

Thanks Craig, you gave me a starting point, now order some parts.

Roy AB7CE

From: AA0ZZ
Sent: Thursday, July 14, 2011 6:37 AM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Re: microR2 and SI570 interfacing

Leroy,

The SN74AC74 is available in 14-pin DIP format (Digikey 296-4342-5-ND) so it's pretty easy to dead-bug that one. Just put it in a socket and attach wires to the socket legs.

The FST3253MX (16-SOIC format) is not available from Digikey but is available from Mouser (512-FST3253MX). I mounted the SOIC part in a 16-pin SOIC "surfboard" (Digikey 161CA-ND) which I super-glued to my ground-plane board. Then it was easy to attach wires to the pads. I built it all "Manhattan style" with connection points made from 1/8" hole punches made from a piece of PC board and super-glued to the ground-plane board. I'll try to get a picture of it.

I've posted the pad layout that I used for this RX front-end (power supply, SN74AC74 and QSD with FST3253MX, and LT6231) in the FILES section of this group. The Si570 control board feeds into this section and the quadrature audio outputs are fed into the MicroR2 audio section.

Best Regards,
-Craig, AA0ZZ

--- In mailto:PPLL-VFO%40yahoogroups.com, "leroy" <lmarion@...> wrote:
>
> I have a micro R2 and a SI570. Schematics provided show
>
> interfacing with FST3225MX/74AC74 circuitry. I looked
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> into getting parts to try to home brew something, and
>
> see the surface mount devices. Anyone came up with
>
> a PC board or some home brew method of making this work?
>
> Thanks, Roy AB7CE
>

59. Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-15 23:18:41 UTC
From: kb1gmx
Topic: 52 Message: 59

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>
> Except that the comparison is wrong on several counts:
>
> 1) Versions of the Si570 can offer a sine wave output.

If you need the square wave to drive counters (90 degree phasing)
then since is less useful.

It's not hard to low pass the output for acceptable sine to drive mixers. It takes only 4 maybe 5 half octave filters to do 3-30mhz.
If the LO is 9mhz higher than the band then it takes fewer maybe 3
for the 12-42mhz range.

> 2) The frequency range extends down to 3.45Mhz.

Actually with a divide by 10 the 10mhz part goes to 1mhz, a divde by 10 is a trivial part (half a 74HCT390). if you need 100khz divide by 100 (use both halves of the 74hct90).

> 3) It is easy to make adjustments to the internal calibration to set
> the frequency accurately, stability is excellent.

Anything that has a micro can be told to put out x when input is set to y. So calibration can be easily done. Further you will likely
(for superhet radio) have the LO at 12.5mhz to receive 3.5 so the micro has to do an offset for the display anyway.

Stability compares to a crystal, for HF thats generally considered very good.

> 4) Yes there is a tuning â□□plopâ□□ but that can be eliminated in software.

There are other ways as well.

> 5) The interface is not tricky just different.

For some of the DDS parts the interface is also different thats
what microprocessors do.

> 6) The phase noise from the Si570 is as good as some professional
> signal generators.

And if the aforementioned /10 is used it improves by 20db.

It is also usable over it's entire range without great variation.

> 7) As he says at the end he just likes DDS i.e. this is his personal
> opinion. What you use is up to you!

> My Si570 8 band TX/RX is almost finished, I will tell more when it is
> working and had some basic testing. I know there are many others using
> similar PPLL-VFOs so there should be some other empirical evidence
> around by now.
>

Some things like 90degree outputs of DDS for phasing gear is a
false trial as its easy to generate (using counters) making hardware
simple.

Testing with a MicroR2 receiver at 40M using a /10 and low pass
filter to replace the built in VFO (si570 running at 70-73mhz) says it's just fine. Doing
it that way the tuning is actually narrow for the Si570 and avoids the plop.

My experiments say for the effort the SI570 offers a lot of simplicity.

There is a case for both but simplicity often wins.

Allison

> Colin - G8FRA/M5FRA
>
> www.m5fra.org.uk
>
>
> ------ Original Message ------
> From: "vpt7388" <vpt7388@...>
> To: PPLL-VFO@yahoogroups.com
> Sent: 14/07/2011 00:55:41
> Subject: [PPLL-VFO] compare a DDS with the SI570
> >Hi all.
> >I have found a very interesting article comparing DDS with SI570.
> >
> >
> >http://www.hanssummers.com/ddssi570.html
> >
> >
> >
> >
> >
> >----------
> >
> >Yahoo! Groups Links
> >
> >http://groups.yahoo.com/group/PPLL-VFO/
> >
> >http://groups.yahoo.com/group/PPLL-VFO/join
> > (Yahoo! ID required)
> >
> >
> >http://docs.yahoo.com/info/terms/
> >
> >

> >
>

60. Re: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 07:32:26 UTC
From: M5FRA - Colin
Topic: 52 Message: 60

I agree with what you say. Like most 'new' ideas many get stuck with what they know and do not see the alternatives.

You said " It's not hard to low pass the output for acceptable sine to drive mixers. It takes only 4 maybe 5 half octave filters to do 3-30mhz. If the LO is 9mhz higher than the band then it takes fewer maybe 3 for the 12-42mhz range."

I have just that, a PPLL that is 9mhz above the operating frequency on 80m-10m. Can you point me to a filter design to clean up the O/P? I have been running the VFO through the RX BPFs using a couple of relays and that works really well but it is an added complication. Any help would be much appreciated.

Colin - G8FRA/M5FRA

61. Cannot get devices

Yahoo group: PPLL-VFO
Date: 2011-07-16 07:36:13 UTC
From: M5FRA - Colin
Topic: 61 Message: 61

I am having problems finding an EU source for the FST3253MX and the LT6231. I can use US suppliers but they are wanting $20 shipping which seems totally excessive for items that will fit in a very small Jiffy bag. Does anybody know of an EU/UK source for these chips?

Thanks.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

62. QEX article

Yahoo group: PPLL-VFO
Date: 2011-07-16 15:17:21 UTC
From: AA0ZZ
Topic: 62 Message: 62

Hi folks,
I have posted a scan (PDF format) of my Si570 QEX article on my web page: www.cbjohn.com/aa0zz . Just below the QEX picture is a link to the original article that was the input to the QEX article. It has the figures in color and in-line with the text. If anyone has corrections, comments or questions, please post them here or let me know.

Best Regards,
-Craig, AA0ZZ

63. Re: [PPLL-VFO] Cannot get devices

Yahoo group: PPLL-VFO
Date: 2011-07-16 15:56:46 UTC
From: P X
Topic: 61 Message: 63

This US supplier has ordinary airmail charges for EU destinations, with no minimum quantity and stocks most popular components for Phasing, QSD and SDR radios !
http://thepartsplace.k5nwa.com/

 You may also try Kees on windy10605@... or K5BCQ@... . He also charges ordinary postal charges !

Various versions of the the SI570 from http://km5h.com/default.aspx

 Enjoy

Peter

From: M5FRA - Colin <m5fra@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: Saturday, July 16, 2011 9:36 AM
Subject: [PPLL-VFO] Cannot get devices

I am having problems finding an EU source for the FST3253MX and the LT6231. I can use US suppliers but they are wanting $20 shipping which seems totally excessive for items that will fit in a very small Jiffy bag. Does anybody know of an EU/UK source for these chips?

Thanks.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

64. Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 17:17:10 UTC
From: kb1gmx
Topic: 52 Message: 64

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>
> I agree with what you say. Like most 'new' ideas many get stuck with
> what they know and do not see the alternatives.
>
> You said " It's not hard to low pass the output for acceptable sine to
> drive mixers. It takes only 4 maybe 5 half octave filters to do
> 3-30mhz. If the LO is 9mhz higher than the band then it takes fewer
> maybe 3 for the 12-42mhz range."
>
> I have just that, a PPLL that is 9mhz above the operating frequency on
> 80m-10m. Can you point me to a filter design to clean up the O/P? I
> have been running the VFO through the RX BPFs using a couple of relays
> and that works really well but it is an added complication. Any help
> would be much appreciated.

If you were here in the USA (maybe it s not an Issue) Id' say get a copy of the ARRL radio amateurs hand book any edition 1965 to current.

A half octave filter is in the name.. It's a filter that has a Fc
of the lowest frequency plus one half that for 12mhz the cutoff
would be 18mhz. The actual filter an be Pi or L section or Pi-L.
The goal is not so much sine wave but to eliminate the 2x,3x and so on harmonics.

So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
filters from..

12.5-18.0mhz filter,
17.5 to 26mhz
26-39mhz

The alternate is run the si570 at 72 to 99mhz and mix it with
a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
filter on the si570 to kill the 120mhz and up harmonics before
the mixer and a second low pass filter after the mixer to
suppress the 40mhz and up. No band switching required. Pay attention to levels going into the DBM use 7dbm from the
60mhz applied to the LO port and -10dbm from the Si570 after
the low pass filter applied to the RF port to get about
-20dbm (with a 3db pad from the IF port of the mixer
and wideband amplifers to get needed levels. Result is
tuning from 2.5 to 29.999 no gaps and fewer plops from
the SI570 as it does fewer freeze/unfreeze at VHF
than HF (the 3500ppm steps are further apart).

One note is the 60mhz osc could easily be 70, 80, 90
or even odd like 64, 66 r even 78,325mhz as the
microprocesser can be told the indicated frequency
is the SI570 freq minus the offset osc and IF.

Allison

> Colin - G8FRA/M5FRA
>

65. Re: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 19:32:29 UTC
From: P X
Topic: 52 Message: 65

Please stop dreaming about theory. Please do something in practice and let us know !!!!!

Peter

From: kb1gmx <kb1gmx@...>
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 7:17 PM
Subject: [PPLL-VFO] Re: compare a DDS with the SI570

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>
> I agree with what you say. Like most 'new' ideas many get stuck with
> what they know and do not see the alternatives.
>
> You said " It's not hard to low pass the output for acceptable sine to
> drive mixers. It takes only 4 maybe 5 half octave filters to do
> 3-30mhz. If the LO is 9mhz higher than the band then it takes fewer
> maybe 3 for the 12-42mhz range."
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> and that works really well but it is an added complication. Any help
> would be much appreciated.

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So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
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12.5-18.0mhz filter,
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The alternate is run the si570 at 72 to 99mhz and mix it with
a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
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the mixer and a second low pass filter after the mixer to
suppress the 40mhz and up. No band switching required. Pay attention to levels going into the DBM use 7dbm from the

60mhz applied to the LO port and -10dbm from the Si570 after
the low pass filter applied to the RF port to get about
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the SI570 as it does fewer freeze/unfreeze at VHF
than HF (the 3500ppm steps are further apart).

One note is the 60mhz osc could easily be 70, 80, 90
or even odd like 64, 66 r even 78,325mhz as the
microprocesser can be told the indicated frequency
is the SI570 freq minus the offset osc and IF.

Allison

> Colin - G8FRA/M5FRA
>

66. The SI570 with the 74AC74

Yahoo group: PPLL-VFO
Date: 2011-07-16 19:42:15 UTC
From: vpt7388
Topic: 66 Message: 66

I have built various SI570 kits, all intended to feed a 74AC74, to feed a switching Tayloe mixer.
In practice, the SI570 LVDS versions had to be levelled by another chip , like the FIN1002,if the 74AC74 was to feed sufficient level to the switching mixers. The SI570 cmos version alone, without amplification, failed. The 74AC74 does divide by four, but the level is insufficient to drive the switching mixers. Amplification is a must !

Practice does not always follows theory or measurements made by sofisticated test equipment !

Peter

67. Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 21:03:17 UTC
From: M5FRA - Colin
Topic: 52 Message: 67

How about an 8 band (80-10m) CW TX/RX based on an Si570 PPLL VFO (PA0KLT). Using relays to switch the RX BPFs into the TX chain and standard LPFs after the PA, it has a very clean output sig and does all I want. Just completing the boxing up so look forward to working you Peter. Next project will be a CW rig as outlined in Craig's QEX article.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "P X" <vpt7388@yahoo.com>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 20:32:29
Subject: Re: [PPLL-VFO] Re: compare a DDS with the SI570
>
>
>Please stop dreaming about theory. Please do something in practice and
>let us know !!!!!
>
>Peter
>
>From: kb1gmx <kb1gmx@...>
>To:PPLL-VFO@yahoogroups.com
>Sent: Saturday, July 16, 2011 7:17 PM
>Subject: [PPLL-VFO] Re: compare a DDS with the SI570
>
>
>
>--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>>
>> I agree with what you say. Like most 'new' ideas many get stuck with
>> what they know and do not see the alternatives.
>>
>> You said " It's not hard to low pass the output for acceptable sine
>to
>> drive mixers. It takes only 4 maybe 5 half octave filters to do
>> 3-30mhz. If the LO is 9mhz higher than the band then it takes fewer
>> maybe 3 for the 12-42mhz range."
>>
>> I have just that, a PPLL that is 9mhz above the operating frequency
>on
>> 80m-10m. Can you point me to a filter design to clean up the O/P? I
>> have been running the VFO through the RX BPFs using a couple of
>relays
>> and that works really well but it is an added complication. Any help

>> would be much appreciated.
>
>If you were here in the USA (maybe it s not an Issue) Id' say get a
>copy of the ARRL radio amateurs hand book any edition 1965 to current.
>
>A half octave filter is in the name.. It's a filter that has a Fc
>of the lowest frequency plus one half that for 12mhz the cutoff
>would be 18mhz. The actual filter an be Pi or L section or Pi-L.
>The goal is not so much sine wave but to eliminate the 2x,3x and so on
>harmonics.
>
>So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
>filters from..
>
>12.5-18.0mhz filter,
>17.5 to 26mhz
>26-39mhz
>
>The alternate is run the si570 at 72 to 99mhz and mix it with
>a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
>filter on the si570 to kill the 120mhz and up harmonics before
>the mixer and a second low pass filter after the mixer to
>suppress the 40mhz and up. No band switching required. Pay attention
>to levels going into the DBM use 7dbm from the
>60mhz applied to the LO port and -10dbm from the Si570 after
>the low pass filter applied to the RF port to get about
>-20dbm (with a 3db pad from the IF port of the mixer
>and wideband amplifers to get needed levels. Result is
>tuning from 2.5 to 29.999 no gaps and fewer plops from
>the SI570 as it does fewer freeze/unfreeze at VHF
>than HF (the 3500ppm steps are further apart).
>
>One note is the 60mhz osc could easily be 70, 80, 90
>or even odd like 64, 66 r even 78,325mhz as the
>microprocesser can be told the indicated frequency
>is the SI570 freq minus the offset osc and IF.
>
>Allison
>
>> Colin - G8FRA/M5FRA
>>
>
>
>
>
>
>
>

68. Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 21:38:31 UTC
From: P X
Topic: 52 Message: 68

I have fed the PA0KLT SI570 kit to the 74ac74, with a FIN1002 leveller chip. It works wonders with a Tayloe switching mixer. ! But the SI570, barefoot cmos version, needs to boost up the level, to switch the switching mixers ! I have also the K5BCQ version, it also works wonders, with a FIN1002!!!

Peter

_____
From: M5FRA - Colin <m5fra@...>
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 11:03 PM
Subject: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

How about an 8 band (80-10m) CW TX/RX based on an Si570 PPLL VFO (PA0KLT). Using relays to switch the RX BPFs into the TX chain and standard LPFs after the PA, it has a very clean output sig and does all I want. Just completing the boxing up so look forward to working you Peter. Next project will be a CW rig as outlined in Craig's QEX article.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "P X" <vpt7388@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 20:32:29
Subject: Re: [PPLL-VFO] Re: compare a DDS with the SI570

>
>
>Please stop dreaming about theory. Please do something in practice and let us know !!!!!
>
>
>Peter
>
>
>
>
>_____
> From: kb1gmx <kb1gmx@...>
>To: PPLL-VFO@yahoogroups.com
>Sent: Saturday, July 16, 2011 7:17 PM
>Subject: [PPLL-VFO] Re: compare a DDS with the SI570
>
>
>
>

>
>--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>>
>> I agree with what you say. Like most 'new' ideas many get stuck with
>> what they know and do not see the alternatives.
>>
>> You said " It's not hard to low pass the output for acceptable sine to
>> drive mixers. It takes only 4 maybe 5 half octave filters to do
>> 3-30mhz. If the LO is 9mhz higher than the band then it takes fewer
>> maybe 3 for the 12-42mhz range."
>>
>> I have just that, a PPLL that is 9mhz above the operating frequency on
>> 80m-10m. Can you point me to a filter design to clean up the O/P? I
>> have been running the VFO through the RX BPFs using a couple of relays
>> and that works really well but it is an added complication. Any help
>> would be much appreciated.
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>
>Allison
>
>> Colin - G8FRA/M5FRA
>>
>
>
>
>
>
>

69. Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 15:14:05 UTC
From: kb1gmx
Topic: 52 Message: 69

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
> Please stop dreaming about theory. Please do something in practice and let us know !!!!!
>
> Peter

No dream. I've built a 0-79mhz signal generator that way as a test and plan to use the same scheme for a multiband radio.

Or are you asking for some one to do the work for you?

Allison

>
>
> _____
> From: kb1gmx <kb1gmx@...>
> To: PPLL-VFO@yahoogroups.com
> Sent: Saturday, July 16, 2011 7:17 PM
> Subject: [PPLL-VFO] Re: compare a DDS with the SI570
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> Â
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> --- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@> wrote:
> >
> > I agree with what you say. Like most 'new' ideas many get stuck with
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> 12.5-18.0mhz filter,
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> is the SI570 freq minus the offset osc and IF.
>
> Allison
>
> > Colin - G8FRA/M5FRA
> >
>

70. Re: The SI570 with the 74AC74

Yahoo group: PPLL-VFO
Date: 2011-07-17 15:22:20 UTC
From: kb1gmx
Topic: 66 Message: 70

--- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
>
> I have built various SI570 kits, all intended to feed a 74AC74, to feed a switching Tayloe mixer.
> In practice, the SI570 LVDS versions had to be levelled by another chip , like the FIN1002,if the 74AC74 was to feed sufficient level to the switching mixers. The SI570 cmos version alone, without amplification, failed. The 74AC74 does divide by four, but the level is insufficient to drive the switching mixers. Amplification is a must !
>
> Practice does not always follows theory or measurements made by sofisticated test equipment !
>
> Peter
>

This is a common problem when mixing 2.7, 3.3 and 5V digital logic.

I had that problem driving 5V 74act74. The problem is the CMOS is 3.3V logic levels and the 5V part wants 5V logic levels, when I used appropriate level translation (discrete mosfet circuit) the problem was solved. One I had the 74act74 running it drove the switching mixer fine (it was also 5V logic). I did find as expected that at 10M (120mhz si570 frequency) the layout was typical of VHF and very high frequency logic and very unhappy with long leads or poor power bypasssing.

Allison

71. Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 17:00:11 UTC
From: Craig Johnson, AA0ZZ
Topic: 52 Message: 71

Peter,
Are you sure? Please be careful. I just checked this again to make sure it is what I remembered. I feed the Si570 output (1.5v square wave) into a pair of 74AC74 flip-flops and the result is at 1/4 the frequency as counted by my oscilloscope. I ran the Si570 from 10 MHz up to 157 MHz.

That being said, I know the SN74AC74 spec sheet says the input should be at least 3.5v for the high so a "shaper" of some sort is a good idea. It doesn't have to be a linear amplifier but just something to "slam" a transistor from cutoff to saturation. I did a computer simulation of a simple circuit with one transistor (a 2N5109) and a couple of resistors and it looks great. Now to build it to make sure. I have 5v coming through a 470 ohm resistor to the collector of the 2N5109 and have the emitter of the 2N5109 grounded. I have a 4.7k resistor from the collector to the base to "self bias" it. Feed the input through a .1u capacitor to the base and you get the output off the collector. A nice square wave nearly "at the rails" (about 4.5v at the high) and it works fine all the way up to 157 MHz (6.4ns period). Other transistors will work as well but a fast one like the 2N5109 is needed for the higher frequencies. Try it.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: P X
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 4:38 PM
Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

I have fed the PA0KLT SI570 kit to the 74ac74, with a FIN1002 leveller chip. It works wonders with a Tayloe switching mixer. ! But the SI570, barefoot cmos version, needs to boost up the level, to switch the switching mixers ! I have also the K5BCQ version, it also works wonders, with a FIN1002!!!

Peter

From: M5FRA - Colin <m5fra@...>
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 11:03 PM
Subject: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

How about an 8 band (80-10m) CW TX/RX based on an Si570 PPLL VFO (PA0KLT). Using relays to switch the RX BPFs into the TX chain and standard LPFs after the PA, it has a very clean output sig and does all I want. Just completing the boxing up so look forward to working you Peter. Next project will be a CW rig as outlined in Craig's QEX article.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "P X" <vpt7388@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 20:32:29
Subject: Re: [PPLL-VFO] Re: compare a DDS with the SI570

Please stop dreaming about theory. Please do something in practice and let us know !!!!!

Peter

From: kb1gmx <kb1gmx@...>
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 7:17 PM
Subject: [PPLL-VFO] Re: compare a DDS with the SI570

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
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> I agree with what you say. Like most 'new' ideas many get stuck with
> what they know and do not see the alternatives.
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> You said " It's not hard to low pass the output for acceptable sine to
> drive mixers. It takes only 4 maybe 5 half octave filters to do
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> maybe 3 for the 12-42mhz range."
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> I have just that, a PPLL that is 9mhz above the operating frequency on
> 80m-10m. Can you point me to a filter design to clean up the O/P? I
> have been running the VFO through the RX BPFs using a couple of relays
> and that works really well but it is an added complication. Any help
> would be much appreciated.

If you were here in the USA (maybe it s not an Issue) Id' say get a copy of the ARRL radio amateurs hand book any edition 1965 to current.

A half octave filter is in the name.. It's a filter that has a Fc
of the lowest frequency plus one half that for 12mhz the cutoff
would be 18mhz. The actual filter an be Pi or L section or Pi-L.
The goal is not so much sine wave but to eliminate the 2x,3x and so on harmonics.

So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
filters from..

12.5-18.0mhz filter,
17.5 to 26mhz
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The alternate is run the si570 at 72 to 99mhz and mix it with
a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
filter on the si570 to kill the 120mhz and up harmonics before
the mixer and a second low pass filter after the mixer to

suppress the 40mhz and up. No band switching required. Pay attention to levels going into the DBM use 7dbm from the
60mhz applied to the LO port and -10dbm from the Si570 after
the low pass filter applied to the RF port to get about
-20dbm (with a 3db pad from the IF port of the mixer
and wideband amplifers to get needed levels. Result is
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the SI570 as it does fewer freeze/unfreeze at VHF
than HF (the 3500ppm steps are further apart).

One note is the 60mhz osc could easily be 70, 80, 90
or even odd like 64, 66 r even 78,325mhz as the
microprocesser can be told the indicated frequency
is the SI570 freq minus the offset osc and IF.

Allison

> Colin - G8FRA/M5FRA
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72. Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 17:35:35 UTC
From: P X
Topic: 52 Message: 72

Talking of level translation, have a look here:
http://py2wm.qsl.br/SDR/Si570/LVDS_TTL_conv.html

Peter

_____
From: "Craig Johnson, AA0ZZ" <aa0zz@...>
To: PPLL-VFO@yahoogroups.com
Sent: Sunday, July 17, 2011 7:00 PM
Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

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just checked this again to make sure it is what I remembered. I feed the
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oscilloscope. I ran the Si570 from 10 MHz up to 157
MHz.

That being said, I know the SN74AC74 spec sheet says the input
should be at least 3.5v for the high so a "shaper" of some sort is a
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something to "slam" a transistor from cutoff to saturation. I did a
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Other transistors will work as well but a fast one like the 2N5109 is needed for
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Best Regards,
-Craig, AA0ZZ

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73. [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 20:33:34 UTC
From: AA0ZZ
Topic: 52 Message: 73

Thanks, Peter.

The BFR92A looks like a good substitute for the 2N5109. It's cheaper too, although it only comes in SMT format. I'm going to order some from Digikey so I can try it out. The simulation looks great.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
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> To: PPLL-VFO@yahoogroups.com
> Sent: Sunday, July 17, 2011 7:00 PM
> Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
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> >From: P X
> >To: PPLL-VFO@yahoogroups.com
> >Sent: Saturday, July 16, 2011 4:38 PM
> >Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
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> <vpt7388@...>
> >To: "PPLL-VFO@yahoogroups.com"
> <PPLL-VFO@yahoogroups.com>

> >Sent: 16/07/2011 20:32:29
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74. [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 23:39:56 UTC
From: kb1gmx
Topic: 52 Message: 74

Hi Craig,

This is common with CMOS, they say 2/3 to 1/3 level will do but
my experience is more along with who made the part and how close to spec. Since I do 2.7 and 1.6V CPUs in embedded development with
fast busses the level translation problem is not unusual. Most of those CPUs are 5V tolerant for inputs but the 5V peripherals usually want to see near rail to rail for best behavior and a 0 to 2..7V signal will not meet that spec. So one brand of 74AC74 may behave and another will act like there is nothing there.

Also CMOS inputs tend to cause high currents if the levels are marginal as the complementary devices are both on. So driving them
rail to rail is usually better behaved.

Besides a FET, MOSFET, or transistor there are several level translator to go from one logic level to another some are even
bidirectional for bus level use like I2C.

Allison

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
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> The goal is not so much sine wave but to eliminate the 2x,3x and so on harmonics.
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> So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
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> The alternate is run the si570 at 72 to 99mhz and mix it with
> a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
> filter on the si570 to kill the 120mhz and up harmonics before

> the mixer and a second low pass filter after the mixer to
> suppress the 40mhz and up. No band switching required. Pay attention to levels going into the DBM use 7dbm from the
> 60mhz applied to the LO port and -10dbm from the Si570 after
> the low pass filter applied to the RF port to get about
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> or even odd like 64, 66 r even 78,325mhz as the
> microprocesser can be told the indicated frequency
> is the SI570 freq minus the offset osc and IF.
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> Allison
>
> > Colin - G8FRA/M5FRA
> >
>

75. Re: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-18 00:01:00 UTC
From: Craig Johnson, AA0ZZ
Topic: 52 Message: 75

Hi Allison,
Thanks for the good advice. My prototype QSD mixer does work, producing quadrature audio out, but I agree that it's best to drive
it at the spec levels.

Since my PIC runs at 5v and the Si570 runs at 3.3v, I implemented bi-directional level translation circuitry on the I2C lines of the
daughtercard. I didn't design the mechanism - it's from the I2C spec - but I changed it to use BS170 MOSFETs and it works great.
It's Figure 7 in my QEX article.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "kb1gmx" <kb1gmx@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, July 17, 2011 6:39 PM
Subject: [PPLL-VFO] Re: compare a DDS with the SI570

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> Hi Craig,
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> This is common with CMOS, they say 2/3 to 1/3 level will do but
> my experience is more along with who made the part and how close to spec. Since I do 2.7 and 1.6V CPUs in embedded development
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> may behave and another will act like there is nothing there.
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>> high) and it works fine all the way up to 157 MHz (6.4ns period). Other transistors will work as well but a fast one like the
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>> From: P X
>> To: PPLL-VFO@yahoogroups.com
>> Sent: Saturday, July 16, 2011 4:38 PM
>> Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
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>> From: M5FRA - Colin <m5fra@...>

>> To: PPLL-VFO@yahoogroups.com
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>> To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
>> Sent: 16/07/2011 20:32:29
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> Yahoo! Groups Links
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76. Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-18 00:43:33 UTC
From: kb1gmx
Topic: 52 Message: 76

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Allison,
> Thanks for the good advice. My prototype QSD mixer does work, producing quadrature audio out, but I agree that it's best to drive
> it at the spec levels.

The problem is one of reproducibility. A different part may behave badly or even one from a different lot. Good levels make that less likely.

> Since my PIC runs at 5v and the Si570 runs at 3.3v, I implemented bi-directional level translation circuitry on the I2C lines of the
> daughtercard. I didn't design the mechanism - it's from the I2C spec - but I changed it to use BS170 MOSFETs and it works great.
> It's Figure 7 in my QEX article.
>

I have seen it. If your driving digital logic on the output side of the Si570 same problems exist and should be dealt with accordingly.
I've used it before on I2C interfaces using the SMT version of the 2n7002.

FYI: when I tried it it also failed for the same reason my solution was to lower the 5V from the FST3225 and the 74ACT74 that Id used
to 3.3 and it started behaving.

Later I went with the already described analog solution (mixdown) to try it with the base microR2 and it worked well. In that cause I had to attenuate the Si570 down to about -10dbm and low pass it before the mixer. Always seems to be too much or not enough. ;)

Allison

> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "kb1gmx" <kb1gmx@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Sunday, July 17, 2011 6:39 PM
> Subject: [PPLL-VFO] Re: compare a DDS with the SI570
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> >> From: P X
> >> To: PPLL-VFO@yahoogroups.com
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> > > Yahoo! Groups Links
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77. Update for W6JL- User Pages

Yahoo group: PPLL-VFO
Date: 2011-07-16 00:07:00 UTC
From: AA0ZZ
Topic: 77 Message: 77

Hi Folks,

I don't know how many of you are aware of the "User Pages" section of my web page but I think you will find this fun to look at. I have been posting write-ups on my web pages from builders of my IQPro VFO and now the Si570 VFO. When builders have gotten something running they have been sending me a write-up and a few pictures and I have been posting them. Builders have made some FANTASTIC projects with the IQPro and now, the first write-up by Don, W6JL, has been updated on the Si570 User Pages. Don was one of the beta testers so he has had a head-start. He was also the original beta tester of my IQPro and the IQ-VFO before that. Don has been using these for several hours every day for many years! Wow! You can find all the write-ups on my web page, www.cbjohn.com/aa0zz , but here's a direct link to Don's Si570 write-up:
http://cbjohn.com/aa0zz/PPLLUsers/W6JL/W6JL.pdf

Hopefully this will spur some of you to do some similar. When you have something to share, please take a few pictures and write a few words describing what you have done. Email it to me (aa0zz@...) and I will fix it up in a PDF file and post it for all to see. I think everyone will appreciate seeing what others are doing. If you have questions you then know who to ask - or you can post the questions here for us to see. We all benefit when we help each other and spur each other on.

Yes, it's already been happening here in this group too. It's great!

Best Regards,
-Craig, AA0ZZ

78. Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-16 22:40:08 UTC
From: Craig Johnson, AA0ZZ
Topic: 52 Message: 78

Peter,

Are you sure? Be careful! I know the SN74AC74 spec sheet says the input should be at least 3.5v for a high
but with the Si570 driving it directly with a 1.5v high square wave DOES WORK! I just tried it again to make sure.
I ran the Si570 all the way up to 157 MHz and my oscilloscope frequency counter indicated that the divide by 4
worked fine.

That being said, it would probably be a good idea to amplify the Si570 signal to drive it harder and meet the spec.
It doesn't have to be a linear amp, of course, but something to drive it hard from saturation to cutoff. I have modeled
a simple circuit with a 2N5109 transistor and a couple of resistors and it looks great. 5v feeding through a 470 ohm
resistor to the collector with the emitter grounded. A 4.7k resistor from the collector to the base biases it. Feed the
signal into the base through a .1u capacitor. Try it! Other transistors may work to but the 2N5109 is a great one
because it's fast.

Best Regards,
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To: PPLL-VFO@yahoogroups.com
Sent: Saturday, July 16, 2011 4:38 PM
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www.m5fra.org.uk

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79. Re: [PPLL-VFO] Cannot get devices

Yahoo group: PPLL-VFO
Date: 2011-07-20 09:39:51 UTC
From: M5FRA - Colin
Topic: 61 Message: 79

To answer my own question use 74CBT3253 which are readily available in
the UK for around £0.25.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "M5FRA - Colin" <m5fra@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 08:36:13
Subject: [PPLL-VFO] Cannot get devices
>
>
>I am having problems finding an EU source for the FST3253MX and the
>LT6231. I can use US suppliers but they are wanting $20 shipping which
>seems totally excessive for items that will fit in a very small Jiffy
>bag. Does anybody know of an EU/UK source for these chips?
>
>Thanks.
>
>Colin - G8FRA/M5FRA
>
>http://www.m5fra.org.uk/
>
>
>
>

80. [PPLL-VFO] Re: compare a DDS with the SI570

Yahoo group: PPLL-VFO
Date: 2011-07-17 20:23:40 UTC
From: AA0ZZ
Topic: 52 Message: 80

Thanks, Peter,

The BFR92A looks like another fast one - a good substitute for the 2N5109. It's much cheaper too, although it's only in SMT format. I'll have to order some so I can try it. The simulation looks great.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, P X <vpt7388@...> wrote:
>
> Talking of level translation, have a look here:
> http://py2wm.qsl.br/SDR/Si570/LVDS_TTL_conv.html
>
> Peter
>
>
>
>
> _____
> From: "Craig Johnson, AA0ZZ" <aa0zz@...>
> To: PPLL-VFO@yahoogroups.com
> Sent: Sunday, July 17, 2011 7:00 PM
> Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
>
>
> Â
> ï»¿
> Peter,
> Are you sure?Â Please be careful. I
> just checked this again to make sure it is what I remembered.Â I feed the
> Si570 output (1.5vÂ square wave) into a pair ofÂ 74AC74 flip-flops and
> the resultÂ isÂ at 1/4 the frequency as counted by my
> oscilloscope.Â I ranÂ the Si570Â from 10 MHz up to 157
> MHz.Â Â
> Â
> That being said, I know the SN74AC74 spec sheet says the input
> should be at least 3.5v forÂ theÂ high so a "shaper" of some sort is a
> good idea.Â Â It doesn't have to be a linear amplifier but just
> something to "slam" a transistor from cutoff to saturation.Â I did a
> computer simulation of a simple circuit with one transistor (a 2N5109) and a
> couple of resistors and it looks great.Â Now to build it to make
> sure.Â Â I have 5v coming through a 470 ohm resistor to the collector
> of the 2N5109 and have the emitter of the 2N5109 grounded.Â I have a 4.7k
> resistor from the collector to the base to "self bias" it.Â Â Feed the
> input through a .1u capacitor to the base and you get the output off the

> collector.Â Â A nice square wave nearly "at the rails"Â (about 4.5v
> at the high) and it works fine all the way up to 157 MHz (6.4ns period).Â
> Other transistors will work as well but a fast one like the 2N5109 is needed for
> the higher frequencies.Â Â Try it.
> Â
> Best Regards,
> -Craig, AA0ZZÂ Â
> Â
> ----- Original Message -----
> >From: P X
> >To: PPLL-VFO@yahoogroups.com
> >Sent: Saturday, July 16, 2011 4:38 PM
> >Subject: Re: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
> >
> >
> >I have fed the PA0KLTÂ SI570Â kit to the 74ac74, with a FIN1002 leveller chip. It
works wonders with a Tayloe switching mixer. ! But the SI570, barefootÂ cmos version,
needsÂ to boost up the level, to switch the switching mixers ! I have also the K5BCQ
version, it also works wonders, with a FIN1002!!!
> >
> >
> >Peter
> >
> >
> >
> >
> >_________________________________
> > From: M5FRA - Colin <m5fra@...>
> >To: PPLL-VFO@yahoogroups.com
> >Sent: Saturday, July 16, 2011 11:03 PM
> >Subject: Re[2]: [PPLL-VFO] Re: compare a DDS with the SI570
> >
> >
> >Â
> >How aboutÂ an 8 band (80-10m) CWÂ TX/RX based on an Si570 PPLL VFO (PA0KLT). Using
relays to switch the RX BPFs into the TX chain and standard LPFs after the PA, it has a
very clean output sig and does all I want. Just completing the boxing upÂ so look forward
to working you Peter.Â Next projectÂ will be aÂ CW rig as outlined in Craig's QEX article.
> >Â
> >Colin - G8FRA/M5FRA
> >Â
> >www.m5fra.org.uk
> >
> >
> >
> >------ Original Message ------
> >From: "P X"
> <vpt7388@...>
> >To: "PPLL-VFO@yahoogroups.com"
> <PPLL-VFO@yahoogroups.com>

> >Sent: 16/07/2011 20:32:29
> >Subject: Re:
> [PPLL-VFO] Re: compare a DDS with the SI570
> >
> >
> >>
> >>
> >>Please stop dreaming about theory. Please do something in practice and let us know
!!!!!
> >>
> >>
> >>Peter
> >>
> >>
> >>
> >>
> >>_________________________________
> >> From: kb1gmx <kb1gmx@...>
> >>To: PPLL-VFO@yahoogroups.com
> >>Sent: Saturday, July 16, 2011 7:17 PM
> >>Subject: [PPLL-VFO] Re: compare a DDS with the SI570
> >>
> >>
> >>Â
> >>
> >>
> >>--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@> wrote:
> >>>
> >>> I agree with what
> you say. Like most 'new' ideas many get stuck with
> >>> what they know
> and do not see the alternatives.
> >>>
> >>> You said " It's not hard
> to low pass the output for acceptable sine to
> >>> drive mixers. It
> takes only 4 maybe 5 half octave filters to do
> >>> 3-30mhz. If the LO
> is 9mhz higher than the band then it takes fewer
> >>> maybe 3 for the
> 12-42mhz range."
> >>>
> >>> I have just that, a PPLL that is 9mhz
> above the operating frequency on
> >>> 80m-10m. Can you point me to a
> filter design to clean up the O/P? I
> >>> have been running the VFO
> through the RX BPFs using a couple of relays
> >>> and that works really
> well but it is an added complication. Any help

> >>> would be much
> appreciated.
> >>
> >>If you were here in the USA (maybe it s not an Issue)
> Id' say get a copy of the ARRL radio amateurs hand book any edition 1965 to
> current.
> >>
> >>A half octave filter is in the name.. It's a filter that has
> a Fc
> >>of the lowest frequency plus one half that for 12mhz the
> cutoff
> >>would be 18mhz. The actual filter an be Pi or L section or
> Pi-L.
> >>The goal is not so much sine wave but to eliminate the 2x,3x and so
> on harmonics.
> >>
> >>So for 3.5 to 30mhz + 9 mhz your looking at a set of LO
> >>filters from..
> >>
> >>12.5-18.0mhz filter,
> >>17.5 to
> 26mhz
> >>26-39mhz
> >>
> >>The alternate is run the si570 at 72 to 99mhz and
> mix it with
> >>a 60mhz crystal osc to get 12 to 39 mhz output. One low pass
> >>filter on the si570 to kill the 120mhz and up harmonics before
> >>the
> mixer and a second low pass filter after the mixer to
> >>suppress the 40mhz
> and up. No band switching required. Pay attention to levels going into the
> DBM use 7dbm from the
> >>60mhz applied to the LO port and -10dbm from the
> Si570 after
> >>the low pass filter applied to the RF port to get about
> >>-20dbm (with a 3db pad from the IF port of the mixer
> >>and wideband
> amplifers to get needed levels. Result is
> >>tuning from 2.5 to 29.999 no
> gaps and fewer plops from
> >>the SI570 as it does fewer freeze/unfreeze at
> VHF
> >>than HF (the 3500ppm steps are further apart).
> >>
> >>One note is
> the 60mhz osc could easily be 70, 80, 90
> >>or even odd like 64, 66 r even
> 78,325mhz as the
> >>microprocesser can be told the indicated frequency

> >>is the SI570 freq minus the offset osc and
> IF.
> >>
> >>Allison
> >>
> >>> Colin -
> G8FRA/M5FRA
> >>>
> >>
> >>
> >>
> >>
> >>
> >>
> >
> >
>

81. Re: [PPLL-VFO] Cannot get devices

Yahoo group: PPLL-VFO
Date: 2011-07-20 18:03:13 UTC
From: P X
Topic: 61 Message: 81

This is really a one stop shop (almost) for most parts we use for Phasing, QSD and SDR radios:
http://thepartsplace.k5nwa.com/

Their shipping charges are very good !

Also, here are some suppliers of bare boards for the SI570 with ordinary mail charges!

http://home.roadrunner.com/~wa6ufq/universal_vfo_controller.html

http://www.wb6dhw.com/Si570/Si570.html

Other interest:

http://www.dspradio.org/df7tv/src11

enjoy

Peter

From: M5FRA - Colin <m5fra@...>
To: PPLL-VFO@yahoogroups.com
Sent: Wednesday, July 20, 2011 11:39 AM
Subject: Re: [PPLL-VFO] Cannot get devices

To answer my own question use 74CBT3253 which are readily available in the UK for around £0.25.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "M5FRA - Colin" <m5fra@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 08:36:13
Subject: [PPLL-VFO] Cannot get devices

>
>
>I am having problems finding an EU source for the FST3253MX and the LT6231. I can use US suppliers but they are wanting $20 shipping which seems totally excessive for items that will fit in a very small Jiffy bag. Does anybody know of an EU/UK source for these chips?
>
>Thanks.
>
>Colin - G8FRA/M5FRA

>
>http://www.m5fra.org.uk/
>
>
>
>

82. Source code

Yahoo group: PPLL-VFO
Date: 2011-07-22 20:32:24 UTC
From: AA0ZZ
Topic: 82 Message: 82

Hi Folks,
Yesterday I pulled the file containing the source code for the PEgen570 application from the FILES section of this group and also from my web site. The HEX file for loading the code into a PIC is still there. I will explain more in a couple of days. In the mean time, to those that have already downloaded it, please do me the courtesy of NOT re-posting it. I'll explain shortly.
Best Regards,
-Craig, AA0ZZ

83. Re[2]: [PPLL-VFO] Cannot get devices

Yahoo group: PPLL-VFO
Date: 2011-07-23 05:28:01 UTC
From: M5FRA - Colin
Topic: 61 Message: 83

Peter, thanks for your reply. Unfortunately it seems that all messages from you have been treated as spam by my ISP so have only just picked them up! I now have all the parts from a UK supplier and have ordered some Micro2pro boards from Kanga. Also have my other project near completion and it is working well.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "P X" <vpt7388@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 16/07/2011 16:56:46
Subject: Re: [PPLL-VFO] Cannot get devices
>
>
>This US supplier has ordinary airmail charges for EU destinations,
>with no minimum quantity and stocks most popular components for
>Phasing, QSD and SDR radios !
>
>http://thepartsplace.k5nwa.com/
>
> You may also try Kees on windy10605@... or K5BCQ@arrl.net . He also charges ordinary postal charges !
>
>Various versions of the the SI570 from http://km5h.com/default.aspx
>
> Enjoy
>
>Peter
>
>From: M5FRA - Colin <m5fra@...>
>To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
>Sent: Saturday, July 16, 2011 9:36 AM
>Subject: [PPLL-VFO] Cannot get devices
>
>
>I am having problems finding an EU source for the FST3253MX and the
>LT6231. I can use US suppliers but they are wanting $20 shipping which
>seems totally excessive for items that will fit in a very small Jiffy
>bag. Does anybody know of an EU/UK source for these chips?
>
>Thanks.
>
>Colin - G8FRA/M5FRA

>
>http://www.m5fra.org.uk/
>
>
>
>
>
>

84. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-26 03:26:55 UTC
From: AA0ZZ
Topic: 82 Message: 84

Hi all,

I said I would provide a little more information about my decision to pull the source code for the PEgen570 application from the FILES section of this forum and also from my web page.

I'm not going to go into a lot of detail but I will say that I have been involved in some extended, semi-public conversations with individuals about how I *owe* it to them and the public in general to release all source code for every project that I develop. As many of you know, I have released the complete source code for many different projects and have helped and encouraged many people make changes to the code. I have done so because I wanted to, not because someone told me I *had* to do so. When I am accosted in public by individuals that don't contribute anything and they tell me that it is my *social responsibility*, I start to revolt. Some of these folks have also told me that software patents are *always evil*, and, as the holder of seven of them, I believe that they can have some value in protecting developer's rights for a limited period of time. I am starting to understand why the vast majority of folks NEVER release their source code.

I've been on vacation this past week - enjoying the beauty of Glacier National Park. While there I spent some time reading a couple of seemingly incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed atheist, Ayn Rand. They are far apart in many fundamental ways and I think Ayn Rand misses the fundamental truth about how God is involved in our lives and is even higher in importance than man's deep thinking and reasoning. Nevertheless, they both have some profound, invaluable truths and they both contributed to my thinking along this line.

I will think it over and some day I may decide to post the source code again. We'll see. In the mean time, to those of you that have already downloaded it, please extend to me the courtesy of not re-posting or re-distributing it here or elsewhere.

Respectfully,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi Folks,
> Yesterday I pulled the file containing the source code for the PEgen570 application from the FILES section of this group and also from my web site. The HEX file for loading the code into a PIC is still there. I will explain more in a couple of days. In the mean time, to those that have already downloaded it, please do me the courtesy of NOT re-posting it. I'll explain shortly.
> Best Regards,
> -Craig, AA0ZZ
>

85. Re: [PPLL-VFO] Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-26 03:54:49 UTC
From: Zack Widup
Topic: 82 Message: 85

I have always considered it a personal decision on the part of the
author of the code. I wonder if the people who demanded the code ever
wrote any themselves?

I have spent countless dozens of hours writing, debugging, fine-tuning
code for a project. It's a lot of work. You probably gleaned from
Atlas Shrugged that by Ayn Rand's philosophy you deserve some exchange
and compensation for your work. But it's up to you if you want to give
it away or charge for it.

I am of the mind that any code I write for ham radio projects be given
away by me. Not so for code I write for work projects. But that's me
and my code, not someone else's. What they do is totally up to them.
It's a LOT of work. And nothing like spending 40-50 hours writing some
firmware, loading it onto a microcontroller, powering it up in the
circuit and having it sit there like a stone. You know what I mean.
:-)

Craig, are you going to sell programmed chips?

73, Zack W9SZ

On 7/25/11, AA0ZZ <aa0zz@...> wrote:
> Hi all,
>
> I said I would provide a little more information about my decision to pull
> the source code for the PEgen570 application from the FILES section of this
> forum and also from my web page.
>
> I'm not going to go into a lot of detail but I will say that I have been
> involved in some extended, semi-public conversations with individuals about
> how I *owe* it to them and the public in general to release all source code
> for every project that I develop. As many of you know, I have released the
> complete source code for many different projects and have helped and
> encouraged many people make changes to the code. I have done so because I
> wanted to, not because someone told me I *had* to do so. When I am accosted
> in public by individuals that don't contribute anything and they tell me
> that it is my *social responsibility*, I start to revolt. Some of these
> folks have also told me that software patents are *always evil*, and, as the
> holder of seven of them, I believe that they can have some value in
> protecting developer's rights for a limited period of time. I am starting
> to understand why the vast majority of folks NEVER release their source
> code.
>
> I've been on vacation this past week - enjoying the beauty of Glacier
> National Park. While there I spent some time reading a couple of seemingly

> incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed
> atheist, Ayn Rand. They are far apart in many fundamental ways and I think
> Ayn Rand misses the fundamental truth about how God is involved in our lives
> and is even higher in importance than man's deep thinking and reasoning.
> Nevertheless, they both have some profound, invaluable truths and they both
> contributed to my thinking along this line.
>
> I will think it over and some day I may decide to post the source code
> again. We'll see. In the mean time, to those of you that have already
> downloaded it, please extend to me the courtesy of not re-posting or
> re-distributing it here or elsewhere.
>
> Respectfully,
> -Craig, AA0ZZ
>
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>>
>> Hi Folks,
>> Yesterday I pulled the file containing the source code for the PEgen570
>> application from the FILES section of this group and also from my web
>> site. The HEX file for loading the code into a PIC is still there. I
>> will explain more in a couple of days. In the mean time, to those that
>> have already downloaded it, please do me the courtesy of NOT re-posting
>> it. I'll explain shortly.
>> Best Regards,
>> -Craig, AA0ZZ
>>
>
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
>
>
>
>

86. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-26 07:57:11 UTC
From: Stephen Farthing
Topic: 82 Message: 86

Craig,

I fully support your decision to pull the source code. In a perfect world the amateur community would respect your decision, after all it is your code, you spent a long time developing it and it is your choice. If you wish you could supply a copy on request for educational purposes but at the end of the day it is your choice.

Here is a sad tale of what can happen if you allow open source and people do not respect the "rules". A friend of mine designed a small microcontroller project and released the source code on his web site. We produced a kit for the project which we sold pretty much at cost as a service to the amateur community. Another amateur copied the design, made a couple of amendments, then passed it to another kit manufacturer as his own work. I am not going to name names here but IMHO the whole thing was deeply unethical and against the spirit of ham radio. It lead to an immense amount of ill feeling between us and the kit manufacturer, who in good faith, had laid out a lot of money on producing the kits. The next time we do a project the source code will not be open and the design will be copyright.

I also know of another amateur who spent a lot of time and effort developing some software which he sold for a nominal fee. Another amateur uploaded the software to his web site and allowed people to download it for free. The net result was the guy that wrote the software never wrote another line of code for amateur use.

At the end of the day Craig the decision is yours and the rest of us should respect it.

73s

Steve...from a cold and rainy England!

--
It is vain to do with more that which can be done with less.

87. Re: [PPLL-VFO] Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-26 08:54:18 UTC
From: M5FRA - Colin
Topic: 82 Message: 87

Craig, it is a sign of the times that some should think they have a 'right' to anything they find on the Internet. I do not write code but did write words for a living. On more than one occasion they were copied and passed off by the thief as their own work. So, I understand why you have decided to pull the source code. My hope is that it does not stop you from continuing the work you are doing which, I for one, really appreciate.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

88. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-26 14:20:34 UTC
From: Bill Oelker
Topic: 82 Message: 88

Craig, I have always enjoyed your projects and the ability to be able to build code and make a project that does something that I want it to do. I am not very good at it and always have admired your ability to build something out of nothing. I have built 3 of your quality kit projects and have learned a bunch on each project and have also enjoyed the pleasure of a resulting programmable electronic device. I appreciate your releasing your projects Source coding as it has helped me understand how and why a device does something. I for one will never be able to do that on my own. So your efforts in sharing what you have created have done some good. So in a sense you have given allot of your your intellectual knowledge willingly and without monetary gain. I hope you will continue to give to all of us fledgelings, that can learn from someone with your experience. I understand your decision to pull the source. However I don't think I or anyone is entitled to your intellectual and knowledge creations. I realize there are allot of folks in this world that do. Thank You for all you do in this Great Hobby of Ours. Bill KN8DMK

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi all,
>
> I said I would provide a little more information about my decision to pull the source code for the PEgen570 application from the FILES section of this forum and also from my web page.
>
> I'm not going to go into a lot of detail but I will say that I have been involved in some extended, semi-public conversations with individuals about how I *owe* it to them and the public in general to release all source code for every project that I develop. As many of you know, I have released the complete source code for many different projects and have helped and encouraged many people make changes to the code. I have done so because I wanted to, not because someone told me I *had* to do so. When I am accosted in public by individuals that don't contribute anything and they tell me that it is my *social responsibility*, I start to revolt. Some of these folks have also told me that software patents are *always evil*, and, as the holder of seven of them, I believe that they can have some value in protecting developer's rights for a limited period of time. I am starting to understand why the vast majority of folks NEVER release their source code.
>
> I've been on vacation this past week - enjoying the beauty of Glacier National Park. While there I spent some time reading a couple of seemingly incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed atheist, Ayn Rand. They are far apart in many fundamental ways and I think Ayn Rand misses the fundamental truth about how God is involved in our lives and is even higher in importance than man's deep thinking and reasoning. Nevertheless, they both have some profound, invaluable truths and they both contributed to my thinking along this line.
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> I will think it over and some day I may decide to post the source code again. We'll see. In the mean time, to those of you that have already downloaded it, please extend to me the courtesy of not re-posting or re-distributing it here or elsewhere.

>
> Respectfully,
> -Craig, AA0ZZ
>
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >
> > Hi Folks,
> > Yesterday I pulled the file containing the source code for the PEgen570 application from the FILES section of this group and also from my web site. The HEX file for loading the code into a PIC is still there. I will explain more in a couple of days. In the mean time, to those that have already downloaded it, please do me the courtesy of NOT re-posting it. I'll explain shortly.
> > Best Regards,
> > -Craig, AA0ZZ
> >
>

89. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 00:58:57 UTC
From: AA0ZZ
Topic: 82 Message: 89

Hi Zack,

--- In PPLL-VFO@yahoogroups.com, Zack Widup <w9sz.zack@...> wrote:
>
> I have always considered it a personal decision on the part of the
> author of the code. I wonder if the people who demanded the code ever
> wrote any themselves?

Probably not ...

> I have spent countless dozens of hours writing, debugging, fine-tuning
> code for a project. It's a lot of work. You probably gleaned from
> Atlas Shrugged that by Ayn Rand's philosophy you deserve some exchange
> and compensation for your work. But it's up to you if you want to give
> it away or charge for it.

Ah - you've read the book too. You know why it hit me between the eyes. Very thought provoking.

It's a great pleasure to deal with most of the folks. That's my payback. I will probably never recover my development costs, let alone anything for my time. Still, I know I have been helped along the way by many other great people who have freely given of their time and expertise. I want to give back also.

> I am of the mind that any code I write for ham radio projects be given
> away by me. Not so for code I write for work projects. But that's me
> and my code, not someone else's. What they do is totally up to them.
> It's a LOT of work. And nothing like spending 40-50 hours writing some
> firmware, loading it onto a microcontroller, powering it up in the
> circuit and having it sit there like a stone. You know what I mean.
> :-)

Do I ever! It's very discouraging and you really have no where to go for help because nobody else really knows the details about what you are doing. You just have to figure out a way to debug it - to get a clue somehwere - and stick to it.

> Craig, are you going to sell programmed chips?
> 73, Zack W9SZ

No, probably not. I will continue to give away the HEX files so folks can always load it into new PICs if they want to.

Best Regards,
-Craig, AA0ZZ

> On 7/25/11, AA0ZZ <aa0zz@...> wrote:
> > Hi all,
> >

> > I said I would provide a little more information about my decision to pull
> > the source code for the PEgen570 application from the FILES section of this
> > forum and also from my web page.
> >
> > I'm not going to go into a lot of detail but I will say that I have been
> > involved in some extended, semi-public conversations with individuals about
> > how I *owe* it to them and the public in general to release all source code
> > for every project that I develop. As many of you know, I have released the
> > complete source code for many different projects and have helped and
> > encouraged many people make changes to the code. I have done so because I
> > wanted to, not because someone told me I *had* to do so. When I am accosted
> > in public by individuals that don't contribute anything and they tell me
> > that it is my *social responsibility*, I start to revolt. Some of these
> > folks have also told me that software patents are *always evil*, and, as the
> > holder of seven of them, I believe that they can have some value in
> > protecting developer's rights for a limited period of time. I am starting
> > to understand why the vast majority of folks NEVER release their source
> > code.
> >
> > I've been on vacation this past week - enjoying the beauty of Glacier
> > National Park. While there I spent some time reading a couple of seemingly
> > incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed
> > atheist, Ayn Rand. They are far apart in many fundamental ways and I think
> > Ayn Rand misses the fundamental truth about how God is involved in our lives
> > and is even higher in importance than man's deep thinking and reasoning.
> > Nevertheless, they both have some profound, invaluable truths and they both
> > contributed to my thinking along this line.
> >
> > I will think it over and some day I may decide to post the source code
> > again. We'll see. In the mean time, to those of you that have already
> > downloaded it, please extend to me the courtesy of not re-posting or
> > re-distributing it here or elsewhere.
> >
> > Respectfully,
> > -Craig, AA0ZZ
> >
> >
> > --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >>
> >> Hi Folks,
> >> Yesterday I pulled the file containing the source code for the PEgen570
> >> application from the FILES section of this group and also from my web
> >> site. The HEX file for loading the code into a PIC is still there. I
> >> will explain more in a couple of days. In the mean time, to those that
> >> have already downloaded it, please do me the courtesy of NOT re-posting
> >> it. I'll explain shortly.
> >> Best Regards,
> >> -Craig, AA0ZZ
> >>
> >

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> > Yahoo! Groups Links
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> >
>

90. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 01:08:13 UTC
From: AA0ZZ
Topic: 82 Message: 90

Hi Steve,

--- In PPLL-VFO@yahoogroups.com, Stephen Farthing <squirrox@...> wrote:
>
> Craig,
>
> I fully support your decision to pull the source code. In a perfect world
> the amateur community would respect your decision, after all it is your
> code, you spent a long time developing it and it is your choice. If you wish
> you could supply a copy on request for educational purposes but at the end
> of the day it is your choice.

Thanks, Steve.

> Here is a sad tale of what can happen if you allow open source
>and people do not respect the "rules". A friend of mine designed
>a small microcontroller project for amateur use.

<snip ...>
That sounds very familiar, Steve. I've had similar things happen but not quite that extreme.

> At the end of the day Craig the decision is yours and the rest of
> us should respect it.
> 73s
> Steve...from a cold and rainy England!

Thanks, Steve.
By the way, it was fun to meet you in the Minneapolis airport on your way to Dayton last year. Quite unexpected, so I hardly recognized you at first. Thanks for all your work with the QRP-ARCI group too.

Best Regards,
-Craig, AA0ZZ

91. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 01:09:51 UTC
From: AA0ZZ
Topic: 82 Message: 91

Hi Colin,

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>
> Craig, it is a sign of the times that some should think they have a
> 'right' to anything they find on the Internet. I do not write code but
> did write words for a living. On more than one occasion they were
> copied and passed off by the thief as their own work. So, I understand
> why you have decided to pull the source code. My hope is that it does
> not stop you from continuing the work you are doing which, I for one,
> really appreciate.
>
> Colin - G8FRA/M5FRA
> www.m5fra.org.uk

Thanks! I still have lots of projects to work on. I'm not giving up.

Best Regards,
-Craig

92. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 01:14:50 UTC
From: AA0ZZ
Topic: 82 Message: 92

Hi Bill,

--- In PPLL-VFO@yahoogroups.com, "Bill Oelker" <boelker@...> wrote:
> Craig, I have always enjoyed your projects and the ability to be able to build code and make a project that does something that I want it to do. I am not very good at it and always have admired your ability to build something out of nothing. I have built 3 of your quality kit projects and have learned a bunch on each project and have also enjoyed the pleasure of a resulting programmable electronic device. I appreciate your releasing your projects Source coding as it has helped me understand how and why a device does something. I for one will never be able to do that on my own. So your efforts in sharing what you have created have done some good. So in a sense you have given allot of your your intellectual knowledge willingly and without monetary gain. I hope you will continue to give to all of us fledgelings, that can learn from someone with your experience. I understand your decision to pull the source. However I don't think I or anyone is entitled to your intellectual and knowledge creations. I realize there are allot of folks in this world that do. Thank You for all you do in this Great Hobby of Ours. Bill KN8DMK
>

Many thanks for your kind words too. No, I'm not giving up.

Best Regards,
-Craig, AA0ZZ

93. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 19:46:16 UTC
From: gm4toe
Topic: 82 Message: 93

Hi Craig,

I totally understand your position and would like to echo all the others giving you thanks for the fine work you did with the piece of programming. I too have had work "ripped off" by the unscrupulous but the option of "sending Louis and the Boys round to sort them out" is no longer morally acceptable!!!

I think I learned more in the hours I spent studying your work than I will ever learn from a library of books. I am still playing with the code, adapting it for my own use, making mistakes and having real fun. There are elements of the coding which I still do not understand (and probably never will) but the struggle continues.

There are those amongst this group who are playing with your code to add different bells and whistles, is there an acceptable way of sharing this work with the group which does not compromise your ownership of the source and the need to keep it out of the public domain?

My heartfelt thanks

Barry GM4TOE

94. Source code is back

Yahoo group: PPLL-VFO
Date: 2011-07-27 22:38:20 UTC
From: AA0ZZ
Topic: 94 Message: 94

Hi all,
I just put the source code back - here in the FILES section and on my web page.

It wsa never my intent to hurt you people - my friends - and I realized that that was what was happening. I was just very frustrated by my recent experiences with certain individuals.

The code was never completely gone anyway - it was always on the QEX site (www.arrl.org/qexfiles). It will remain now.

Best Regards,
-Craig, AA0ZZ

95. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 22:53:07 UTC
From: kb1gmx
Topic: 82 Message: 95

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi all,
>
> I said I would provide a little more information about my decision to pull the source code for the PEgen570 application from the FILES section of this forum and also from my web page.
>
> I'm not going to go into a lot of detail but I will say that I have been involved in some extended, semi-public conversations with individuals about how I *owe* it to them and the public in general to release all source code for every project that I develop. As many of you know, I have released the complete source code for many different projects and have helped and encouraged many people make changes to the code. I have done so because I wanted to, not because someone told me I *had* to do so. When I am accosted in public by individuals that don't contribute anything and they tell me that it is my *social responsibility*, I start to revolt. Some of these folks have also told me that software patents are *always evil*, and, as the holder of seven of them, I believe that they can have some value in protecting developer's rights for a limited period of time. I am starting to understand why the vast majority of folks NEVER release their source code.
>
> I've been on vacation this past week - enjoying the beauty of Glacier National Park. While there I spent some time reading a couple of seemingly incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed atheist, Ayn Rand. They are far apart in many fundamental ways and I think Ayn Rand misses the fundamental truth about how God is involved in our lives and is even higher in importance than man's deep thinking and reasoning. Nevertheless, they both have some profound, invaluable truths and they both contributed to my thinking along this line.
>
> I will think it over and some day I may decide to post the source code again. We'll see. In the mean time, to those of you that have already downloaded it, please extend to me the courtesy of not re-posting or re-distributing it here or elsewhere.
>
> Respectfully,
> -Craig, AA0ZZ

I support whatever choice you make. Please, keep the kill
projects coming.

I've been on the net since before the "green card" and WWW...
I've encountered it before as well. I've even had a rather
annoying fancophone tell me I could not leave the tech group
as I was a valuable resource, his wording was more like I was property and I "owe". Adults, they not be.

Allison

>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >
> > Hi Folks,
> > Yesterday I pulled the file containing the source code for the PEgen570 application from the FILES section of this group and also from my web site. The HEX file for loading the code into a PIC is still there. I will explain more in a couple of days. In the mean time, to those that have already downloaded it, please do me the courtesy of NOT re-posting it. I'll explain shortly.
> > Best Regards,
> > -Craig, AA0ZZ
> >
>

96. Re: [PPLL-VFO] Source code is back

Yahoo group: PPLL-VFO
Date: 2011-07-27 23:31:16 UTC
From: Dave Mallery
Topic: 94 Message: 96

many thanks, craig...

i think some folks don't understand your code is yours and you don't release
it under gpl or other license.

thanks for putting it back... i had just received my si570 kit.

73

dave

On Wed, Jul 27, 2011 at 3:38 PM, AA0ZZ <aa0zz@...> wrote:

> **
>
>
> Hi all,
> I just put the source code back - here in the FILES section and on my web
> page.
>
> It wsa never my intent to hurt you people - my friends - and I realized
> that that was what was happening. I was just very frustrated by my recent
> experiences with certain individuals.
>
> The code was never completely gone anyway - it was always on the QEX site (
> www.arrl.org/qexfiles). It will remain now.
>
> Best Regards,
> -Craig, AA0ZZ
>
>
>
>

--
Dave Mallery, K5EN (ubuntu linux 11.04)
PO Box 416; Gold Beach, OR 97444

no gates...
no windows!
free at last!
linux counter #64628 (since 1997)

"People aren't as dumb as Microsoft needs them to be."
--PJ, May 2007

97. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-07-27 23:34:29 UTC
From: kb1gmx
Topic: 82 Message: 97

--- In PPLL-VFO@yahoogroups.com, "kb1gmx" <kb1gmx@...> wrote:
>
>
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >
> > Hi all,
> >
> > I said I would provide a little more information about my decision to pull the source code for the PEgen570 application from the FILES section of this forum and also from my web page.
> >
> > I'm not going to go into a lot of detail but I will say that I have been involved in some extended, semi-public conversations with individuals about how I *owe* it to them and the public in general to release all source code for every project that I develop. As many of you know, I have released the complete source code for many different projects and have helped and encouraged many people make changes to the code. I have done so because I wanted to, not because someone told me I *had* to do so. When I am accosted in public by individuals that don't contribute anything and they tell me that it is my *social responsibility*, I start to revolt. Some of these folks have also told me that software patents are *always evil*, and, as the holder of seven of them, I believe that they can have some value in protecting developer's rights for a limited period of time. I am starting to understand why the vast majority of folks NEVER release their source code.
> >
> > I've been on vacation this past week - enjoying the beauty of Glacier National Park. While there I spent some time reading a couple of seemingly incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed atheist, Ayn Rand. They are far apart in many fundamental ways and I think Ayn Rand misses the fundamental truth about how God is involved in our lives and is even higher in importance than man's deep thinking and reasoning. Nevertheless, they both have some profound, invaluable truths and they both contributed to my thinking along this line.
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> >
> > Respectfully,
> > -Craig, AA0ZZ
>
> I support whatever choice you make. Please, keep the kill
> projects coming.
>

DRAT! that was supposed to be KILLER as in really sweet projects.

I need more sleep.

Allison

> I've been on the net since before the "green card" and WWW...
> I've encountered it before as well. I've even had a rather
> annoying fancophone tell me I could not leave the tech group
> as I was a valuable resource, his wording was more like I was property and I "owe".
Adults, they not be.
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>
> Allison
>
>
> >
> > --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> > >
> > > Hi Folks,
> > > Yesterday I pulled the file containing the source code for the PEgen570 application
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time, to those that have already downloaded it, please do me the courtesy of NOT re-posting
it. I'll explain shortly.
> > > Best Regards,
> > > -Craig, AA0ZZ
> > >
> >
>

98. Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-29 15:34:34 UTC
From: vpt7388
Topic: 98 Message: 98

Hi all.
I am not too technical about programming.
Can I program an Atmel AVR processor with a PIC programmer, using the PonyProg AVR programming software ??

Peter

99. Re: [PPLL-VFO] Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-29 16:03:09 UTC
From: Stephen Farthing
Topic: 98 Message: 99

Peter,

I do not believe you can use a PIC programmer to program an AVR. There are all sorts of AVR devices so to advise you we need to know what device you are wishing to program and what sort of interface your PC has (USB, Serial or parallel).

For the 8 bit AVR series I use an ATMEL AVR ISPMk2 which uses a USB interface with the PC. I made up a target vboard using a ZIF socket so I can program the various chips some of which have 8 pins, others have more pins. I connect the programmer to the board via a header. There is an excellent set of tutorials at http://www.sparkfun.com/tutorials. Click on the link "Beginning Embedded Electronics" and it will talk you through what you need to know to get started with AVR 8 bit processors,

I program my stand alone AVR projects in C using the WinAVR toolset and AVR studio all of which are free. There are a number of homebrew programmer designs on the net but I don't have any experience of these.

Hope this helps,

73s Steve G0XAR

On 29 July 2011 16:34, vpt7388 <vpt7388@...> wrote:

> **
>
>
> Hi all.
> I am not too technical about programming.
> Can I program an Atmel AVR processor with a PIC programmer, using the
> PonyProg AVR programming software ??
>
> Peter
>
>
>

--
It is vain to do with more that which can be done with less.

100. Re: [PPLL-VFO] Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-29 16:24:59 UTC
From: Zack Widup
Topic: 98 Message: 100

I think you'd have to rewrite all the code in Atmel language. You'd also need a programmer that does Atmel chips if doing it directly, I think.

I could be wrong. I've never done that before.

73, Zack W9SZ

On Fri, Jul 29, 2011 at 10:34 AM, vpt7388 <vpt7388@...> wrote:

> Hi all.
> I am not too technical about programming.
> Can I program an Atmel AVR processor with a PIC programmer, using the
> PonyProg AVR programming software ??
>
> Peter
>
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> Yahoo! Groups Links
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101. Re: [PPLL-VFO] Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-29 16:44:56 UTC
From: Stephen Farthing
Topic: 98 Message: 101

Zack,

You are right. Generally each type of processor has a different internal setup so the low level code (machine code) is specific to that type of processor. In non computer speak this means that code that works on a Pic will not work on an Atmel and code that works on a Pic. And as each processor type is different they each a different hardware programmer to load the code into the processor.

However if you are starting out learning to program from scratch I would suggest instead of learning processor specific machine/assembler code you learn a high level language like C. C is available for just about any processor currently available. In a way C is like having a set of spanners, files, screwdrivers and other workshop tools that enable you to work on any machine from a lawnmower to a truck. So if you know C you can program any sort of processor without having to know too much about how it works, Though you do have to know some stuff like what pins do what in I/O terms and how to read/write to them. And there is always going to be someone who will say that for pure performance you need to program in machine code/assembler. Personally that has never been my experience.

73s Steve

On 29 July 2011 17:24, Zack Widup <w9sz.zack@...> wrote:

> **
>
>
> I think you'd have to rewrite all the code in Atmel language. You'd also
> need a programmer that does Atmel chips if doing it directly, I think.
>
> I could be wrong. I've never done that before.
>
> 73, Zack W9SZ
>
>
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>> ------------------------------------
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>> Yahoo! Groups Links
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It is vain to do with more that which can be done with less.

102. Re: [PPLL-VFO] Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-29 17:54:32 UTC
From: Zack Widup
Topic: 98 Message: 102

I've been using an STK-500 for AVR's. I've been thinking of getting an STK-600 one of these days. My only complaint about the STK-500 is that the sockets on the board are not ZIF sockets. I made adaptors for them using ZIF sockets.

I like programming in assembler because that's what I first learned. I'm picking up C but still write quite a bit in assembler as a personal preference. But that's just me.
:-)

73, Zack W9SZ

On Fri, Jul 29, 2011 at 11:44 AM, Stephen Farthing <squirrox@...>wrote:

>
>
> Zack,
>
> You are right. Generally each type of processor has a different internal
> setup so the low level code (machine code) is specific to that type of
> processor. In non computer speak this means that code that works on a Pic
> will not work on an Atmel and code that works on a Pic. And as each
> processor type is different they each a different hardware programmer to
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>
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> suggest instead of learning processor specific machine/assembler code you
> learn a high level language like C. C is available for just about any
> processor currently available. In a way C is like having a set of spanners,
> files, screwdrivers and other workshop tools that enable you to work on any
> machine from a lawnmower to a truck. So if you know C you can program any
> sort of processor without having to know too much about how it works, Though
> you do have to know some stuff like what pins do what in I/O terms and how
> to read/write to them. And there is always going to be someone who will say
> that for pure performance you need to program in machine code/assembler.
> Personally that has never been my experience.
>
> 73s Steve
>
>
> On 29 July 2011 17:24, Zack Widup <w9sz.zack@...> wrote:
>
>> **
>>
>>
>> I think you'd have to rewrite all the code in Atmel language. You'd also

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>> I could be wrong. I've never done that before.
>>
>> 73, Zack W9SZ
>>
>>
>> On Fri, Jul 29, 2011 at 10:34 AM, vpt7388 <vpt7388@...> wrote:
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> --
> It is vain to do with more that which can be done with less.
>
>
>

103. Re: Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-30 15:33:13 UTC
From: AA0ZZ
Topic: 98 Message: 103

Peter,

--- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
>
> Hi all.
> I am not too technical about programming.
> Can I program an Atmel AVR processor with a PIC programmer, using the PonyProg AVR programming software ??
> Peter
>
I also am not quite sure exactly what you are asking but you have already been given some good advice. PIC and ATMEL programmers are completely different as are the software applications that assemble (or compile) the programmer's instructions and the applications that move the code from the PC to the micro.

I am not sure if you are thinking that you want to port the PEgen570 application to an ATMEL. While that is certainly possible it's a huge job. I'm sure that there is no ATMEL processor that would fit into the 18-pin DIP socket either, so you would have to make a new control board of some sort.

The advice about programming in "C" is also good. BASIC is another viable option, although I don't know of any inexpensive BASIC compilers for the PIC. (If someone knows of one, please let me know. The cheapest I can find is about $150.) Most serious applications are written in C or C++ these days, for speed in development ($$) as well as maintenance/support cost.

That being said, there still are reasons to know how to program microcontrollers in the native assembler languages. Yes, the instructions are different for each family (PIC, ATMEL, etc) - and to a lesser extent within the families - but you can move within the families without too much difficulty. Each micro in the family will have different options that you always have to understand because you will have to add instructions to enable the options you want and disable those that you don't want. This is true whether you program in assembler or C or C++ or BASIC. You always have to understand the architectures.

The reason why some knowledge of assembler programming may still be needed is because you sometimes have to do something special that isn't available via a compiler library function call. For example, in the PEgen570 I needed to do a 40-bit by 40-bit division and I needed the result to be a 10 bit integer plus 28-bits of fraction. (These bytes are required parameters that the Si570 needs to generate the exact, desired frequency.) I had to work this by first analyzing a standard 32 bit by 32 bit integer division algorithm, working it out on paper in binary (ones and zeros only), dividing the "old fashioned way" by subtracting and shifting. However, the standard division algorithms divide two integers (whole numbers) and end up with another integer with the fraction truncated. I had to extend the standard integer algorithm, using available PIC registers, to force it to continue the division operation after the integer was determined to calculate the fraction bits. I really wanted the end result to be positioned within the bytes such that they could

be loaded directly into the Si570 registers to make the algorithm fast. This operation is performed on every frequency change so it will be noticeable if the algorithm is not efficient.

Getting to understand any microcontroller's architecture is essential for any programmer. That's the purpose of the free Elmer 160 course that goes along with my PIC-EL board. The complete PEgen570 application was developed and debugged on my PIC-EL board. That was an easy, fun way to do it.

Best Regards,
-Craig, AA0ZZ

104. Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 18:15:51 UTC
From: ag4qc
Topic: 104 Message: 104

I guess it might just be me and old age. But when I first built the project (Control & Daughter board) I swear it just displayed the frequency. There was nothing on the second line and also nothing before the the frequency. That was perfect as I'm using this as a signal generator. Then I read about the options of Upper/Lower sideband and so on. So I pressed PB4 and all the sudden now I can't get rid of the (U/L/-/+) in front of the frequency and also now I have the debug information on the second line. Like I said, maybe it was always there and it's just me. But it does bring up the question; Is there a way to say I don't want upper/lower and so on to be displayed? Maybe a factory reset or something? Now that the source is back on the site, I know I can burn another version of the PIC, but I hate to modify anything and then have to perpetuate the changes anytime there is a bug fix or update.

Anyone have a suggestion?
73
Joe Loucka AG4QC

105. Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 18:55:17 UTC
From: AA0ZZ
Topic: 104 Message: 105

H Joe,

--- In PPLL-VFO@yahoogroups.com, "ag4qc" <ag4qc@...> wrote:
>
> I guess it might just be me and old age. But when I first built the project (Control & Daughter board) I swear it just displayed the frequency. There was nothing on the second line and also nothing before the the frequency. That was perfect as I'm using this as a signal generator. Then I read about the options of Upper/Lower sideband and so on. So I pressed PB4 and all the sudden now I can't get rid of the (U/L/-/+) in front of the frequency and also now I have the debug information on the second line. Like I said, maybe it was always there and it's just me. But it does bring up the question; Is there a way to say I don't want upper/lower and so on to be displayed? Maybe a factory reset or something? Now that the source is back on the site, I know I can burn another version of the PIC, but I hate to modify anything and then have to perpetuate the changes anytime there is a bug fix or update.
>
> Anyone have a suggestion?
> 73
> Joe Loucka AG4QC
>
The first position of line 1 of the LCD always contains one of the four symbols (U/L/+/-). It starts out with a + in that position. I just loaded a fresh copy into a PIC to make sure. It can only be removed with a software change.

Best Regards,
-Craig, AA0ZZ

106. Re: [PPLL-VFO] Re: Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-30 19:53:29 UTC
From: Zack Widup
Topic: 98 Message: 106

I did something similar with the AD9835 and AD9850. I took some PIC code I'd written for the AD9835 and rewrote it for an AVR. It was a lot of work but I finally got it to work. You pretty much have to start from scratch with the AVR. I did it all in AVR assembler.

I don't think I'd want to do that too often. Although the AVR's have several advantages over the PIC's, it's probably not worth it in most cases to migrate an existing PIC program.

73, Zack W9SZ

On 7/30/11, AA0ZZ <aa0zz@...> wrote:
> Peter,
>
> --- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
>>
>> Hi all.
>> I am not too technical about programming.
>> Can I program an Atmel AVR processor with a PIC programmer, using the
>> PonyProg AVR programming software ??
>> Peter
>>
> I also am not quite sure exactly what you are asking but you have already
> been given some good advice. PIC and ATMEL programmers are completely
> different as are the software applications that assemble (or compile) the
> programmer's instructions and the applications that move the code from the
> PC to the micro.
>
> I am not sure if you are thinking that you want to port the PEgen570
> application to an ATMEL. While that is certainly possible it's a huge job.
> I'm sure that there is no ATMEL processor that would fit into the 18-pin DIP
> socket either, so you would have to make a new control board of some sort.
>
>
> The advice about programming in "C" is also good. BASIC is another viable
> option, although I don't know of any inexpensive BASIC compilers for the
> PIC. (If someone knows of one, please let me know. The cheapest I can find
> is about $150.) Most serious applications are written in C or C++ these
> days, for speed in development ($$) as well as maintenance/support cost.
>
> That being said, there still are reasons to know how to program
> microcontrollers in the native assembler languages. Yes, the instructions
> are different for each family (PIC, ATMEL, etc) - and to a lesser extent
> within the families - but you can move within the families without too much
> difficulty. Each micro in the family will have different options that you
> always have to understand because you will have to add instructions to

> enable the options you want and disable those that you don't want. This is
> true whether you program in assembler or C or C++ or BASIC. You always have
> to understand the architectures.
>
> The reason why some knowledge of assembler programming may still be needed
> is because you sometimes have to do something special that isn't available
> via a compiler library function call. For example, in the PEgen570 I needed
> to do a 40-bit by 40-bit division and I needed the result to be a 10 bit
> integer plus 28-bits of fraction. (These bytes are required parameters that
> the Si570 needs to generate the exact, desired frequency.) I had to work
> this by first analyzing a standard 32 bit by 32 bit integer division
> algorithm, working it out on paper in binary (ones and zeros only), dividing
> the "old fashioned way" by subtracting and shifting. However, the standard
> division algorithms divide two integers (whole numbers) and end up with
> another integer with the fraction truncated. I had to extend the standard
> integer algorithm, using available PIC registers, to force it to continue
> the division operation after the integer was determined to calculate the
> fraction bits. I really wanted the end result to be positioned within the
> bytes such that they could be loaded directly into the Si570 registers to
> make the algorithm fast. This operation is performed on every frequency
> change so it will be noticeable if the algorithm is not efficient.
>
> Getting to understand any microcontroller's architecture is essential for
> any programmer. That's the purpose of the free Elmer 160 course that goes
> along with my PIC-EL board. The complete PEgen570 application was developed
> and debugged on my PIC-EL board. That was an easy, fun way to do it.
>
> Best Regards,
> -Craig, AA0ZZ
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> Yahoo! Groups Links
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107. Re: [PPLL-VFO] Re: Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:12:37 UTC
From: Stephen Farthing
Topic: 98 Message: 107

Hi Guys,

One thing I forgot to say was if you write things in C carefully enough you can end up with a lot of common code that will run on any processor This approach is OK for a lot of things but not when you want to use a specific feature of one type of processor. In that case you may have to resort to assembler or processor specific libraries.

Personally I stick to C and Arduino when writing code for microcontrollers. I like an English or Maths like syntax and my brain is not big enough to cope with machine code or assembler. And I never, ever program in BASIC!

73s Steve G0XAR

On 30 July 2011 20:53, Zack Widup <w9sz.zack@...> wrote:

> **
>
>
> I did something similar with the AD9835 and AD9850. I took some PIC
> code I'd written for the AD9835 and rewrote it for an AVR. It was a
> lot of work but I finally got it to work. You pretty much have to
> start from scratch with the AVR. I did it all in AVR assembler.
>
> I don't think I'd want to do that too often. Although the AVR's have
> several advantages over the PIC's, it's probably not worth it in most
> cases to migrate an existing PIC program.
>
> 73, Zack W9SZ
>
>
> On 7/30/11, AA0ZZ <aa0zz@...> wrote:
> > Peter,
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> > --- In PPLL-VFO@yahoogroups.com, "vpt7388" <vpt7388@...> wrote:
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> >> Hi all.
> >> I am not too technical about programming.
> >> Can I program an Atmel AVR processor with a PIC programmer, using the
> >> PonyProg AVR programming software ??
> >> Peter
> >>
> > I also am not quite sure exactly what you are asking but you have already
> > been given some good advice. PIC and ATMEL programmers are completely
> > different as are the software applications that assemble (or compile) the
> > programmer's instructions and the applications that move the code from

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> > PC to the micro.
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> > I am not sure if you are thinking that you want to port the PEgen570
> > application to an ATMEL. While that is certainly possible it's a huge
> job.
> > I'm sure that there is no ATMEL processor that would fit into the 18-pin
> DIP
> > socket either, so you would have to make a new control board of some
> sort.
> >
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> > option, although I don't know of any inexpensive BASIC compilers for the
> > PIC. (If someone knows of one, please let me know. The cheapest I can
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> > is about $150.) Most serious applications are written in C or C++ these
> > days, for speed in development ($$) as well as maintenance/support cost.
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> > difficulty. Each micro in the family will have different options that you
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> > enable the options you want and disable those that you don't want. This
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> > true whether you program in assembler or C or C++ or BASIC. You always
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> > The reason why some knowledge of assembler programming may still be
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> > is because you sometimes have to do something special that isn't
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> > to do a 40-bit by 40-bit division and I needed the result to be a 10 bit
> > integer plus 28-bits of fraction. (These bytes are required parameters
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> > the Si570 needs to generate the exact, desired frequency.) I had to work
> > this by first analyzing a standard 32 bit by 32 bit integer division
> > algorithm, working it out on paper in binary (ones and zeros only),
> dividing
> > the "old fashioned way" by subtracting and shifting. However, the
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> > division algorithms divide two integers (whole numbers) and end up with
> > another integer with the fraction truncated. I had to extend the standard
> > integer algorithm, using available PIC registers, to force it to continue

> > the division operation after the integer was determined to calculate the
> > fraction bits. I really wanted the end result to be positioned within the
> > bytes such that they could be loaded directly into the Si570 registers to
> > make the algorithm fast. This operation is performed on every frequency
> > change so it will be noticeable if the algorithm is not efficient.
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> > Getting to understand any microcontroller's architecture is essential for
> > any programmer. That's the purpose of the free Elmer 160 course that goes
> > along with my PIC-EL board. The complete PEgen570 application was
> developed
> > and debugged on my PIC-EL board. That was an easy, fun way to do it.
> >
> > Best Regards,
> > -Craig, AA0ZZ
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It is vain to do with more that which can be done with less.

108. Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:13:07 UTC
From: AA0ZZ
Topic: 104 Message: 108

Joe,

If you have the equipment to program a new PIC, I will work on a new version of the code for you that does not display the character in position 1 of line 1. It will start out in "U" instead of "+" so no CW offset is in effect and the frequency displayed will the frequency generated by the Si570, regardless of the state of the Transmit/Receive header. Note that if you change it via the menu you will no longer be able to tell what mode it is in. You will have to restore to the original by loading a new copy.

Let me know if you want this.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> H Joe,
>
> --- In PPLL-VFO@yahoogroups.com, "ag4qc" <ag4qc@> wrote:
> >
> > I guess it might just be me and old age. But when I first built the project (Control & Daughter board) I swear it just displayed the frequency. There was nothing on the second line and also nothing before the the frequency. That was perfect as I'm using this as a signal generator. Then I read about the options of Upper/Lower sideband and so on. So I pressed PB4 and all the sudden now I can't get rid of the (U/L/-/+) in front of the frequency and also now I have the debug information on the second line. Like I said, maybe it was always there and it's just me. But it does bring up the question; Is there a way to say I don't want upper/lower and so on to be displayed? Maybe a factory reset or something? Now that the source is back on the site, I know I can burn another version of the PIC, but I hate to modify anything and then have to perpetuate the changes anytime there is a bug fix or update.
> >
> > Anyone have a suggestion?
> > 73
> > Joe Loucka AG4QC
> >
> The first position of line 1 of the LCD always contains one of the four symbols (U/L/+/-). It starts out with a + in that position. I just loaded a fresh copy into a PIC to make sure. It can only be removed with a software change.
>
> Best Regards,
> -Craig, AA0ZZ
>

109. Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:15:58 UTC
From: ag4qc
Topic: 104 Message: 109

Ah, okay.. Well I guess I missed it.. But the second line is always there also? Hard to believe I thought the second line was blank in the beginning also. Hmm.. I guess I'll turn off debugging and make the software changes for the symbols.

Thanks for a really nice product,

Joe

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> H Joe,
>
> --- In PPLL-VFO@yahoogroups.com, "ag4qc" <ag4qc@> wrote:
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>
> Best Regards,
> -Craig, AA0ZZ
>

110. Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:20:57 UTC
From: ag4qc
Topic: 104 Message: 110

Yeah, I program the 16F628's all the time. So I can make the changes. Don't worry about me. I just thought I missed an option in the menu or something. It seems that a blank along with the other symbols made sense.

Joe

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Joe,
>
> If you have the equipment to program a new PIC, I will work on a new version of the code for you that does not display the character in position 1 of line 1. It will start out in "U" instead of "+" so no CW offset is in effect and the frequency displayed will the frequency generated by the Si570, regardless of the state of the Transmit/Receive header. Note that if you change it via the menu you will no longer be able to tell what mode it is in. You will have to restore to the original by loading a new copy.
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> Let me know if you want this.
>
> Best Regards,
> -Craig, AA0ZZ
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> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
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> > H Joe,
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> > Best Regards,
> > -Craig, AA0ZZ
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>

111. Re: [PPLL-VFO] Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:21:57 UTC
From: Craig Johnson, AA0ZZ
Topic: 104 Message: 111

Joe,
Sorry, not being able to turn off DEBUG mode was a bug in version 7.5. Once it got turned on it couldn't be turned off. It is
fixed in the latest version.

Again, if you have the equipment to burn a new PIC you can pick up the latest HEX file from the FILES section or from my web page
and burn a new one. If you don't, let me or Bill Kelsey know and we can get you a new PIC.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ag4qc" <ag4qc@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Saturday, July 30, 2011 3:15 PM
Subject: [PPLL-VFO] Re: Frequency display

> Ah, okay.. Well I guess I missed it.. But the second line is always there also? Hard to believe I thought the second line was
> blank in the beginning also. Hmm.. I guess I'll turn off debugging and make the software changes for the symbols.
>
> Thanks for a really nice product,
>
> Joe
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> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
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>> Best Regards,
>> -Craig, AA0ZZ
>>
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112. Re: [PPLL-VFO] Re: Frequency display

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:23:28 UTC
From: Craig Johnson, AA0ZZ
Topic: 104 Message: 112

Joe,
Good. I'll work on a new version without the DEBUG mode bug and with that character turned off. I'll let you know.
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ag4qc" <ag4qc@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Saturday, July 30, 2011 3:20 PM
Subject: [PPLL-VFO] Re: Frequency display

> Yeah, I program the 16F628's all the time. So I can make the changes. Don't worry about me. I just thought I missed an option in
> the menu or something. It seems that a blank along with the other symbols made sense.
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> Joe
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
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>> Joe,
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>> character in position 1 of line 1. It will start out in "U" instead of "+" so no CW offset is in effect and the frequency
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>> change it via the menu you will no longer be able to tell what mode it is in. You will have to restore to the original by
>> loading a new copy.
>>
>> Let me know if you want this.
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>> Best Regards,
>> -Craig, AA0ZZ
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>>
>> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
>> >
>> > H Joe,
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>> > >
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>> > Best Regards,
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113. Re: Frequency display - new version 7;7a for AG5QC

Yahoo group: PPLL-VFO
Date: 2011-07-30 20:52:37 UTC
From: AA0ZZ
Topic: 104 Message: 113

Joe,

I have posted a new version for you - v7.7a - in the FILES section. Source code and HEX file. I have tested it in a simulator and it should work OK. Note that it starts out in "U" mode. Let me know.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
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> Joe,
> Good. I'll work on a new version without the DEBUG mode bug and with that character turned off. I'll let you know.
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>

114. Re: Frequency display - new version 7;7a for AG5QC

Yahoo group: PPLL-VFO
Date: 2011-07-31 06:20:43 UTC
From: ag4qc
Topic: 104 Message: 114

Craig,
I just loaded the hex code and it works great. I don't even seem to have the +/-/L/U options any more. It looks like I only have the 1-4 Menu options, which is great. That and the debug data is also gone. So for my use, it's all good. Man, talk about customer service, you are a breath of fresh air!

Thank you again,

- Joe AG4QC

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
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> Best Regards,
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>

115. Re: [PPLL-VFO] Re: Programming AVR

Yahoo group: PPLL-VFO
Date: 2011-07-31 10:06:00 UTC
From: P X
Topic: 98 Message: 115

Hi all,

Thanks for the feedback.
I think the best thing to do to start with PIC and AVR is to try the Picaxe, which is bootleg with ordinary basic language
http://www.rev-ed.co.uk/picaxe/

Must say, it has some restrictions, when compared to assembly language. However, for a new comer, it should be ok

http://www.dspradio.org/df7tv/src11

Thanks folks

Peter

116. Re: [PPLL-VFO] Re: Frequency display - new version 7.7a for AG5QC

Yahoo group: PPLL-VFO
Date: 2011-07-31 12:53:11 UTC
From: Craig Johnson, AA0ZZ
Topic: 116 Message: 116

Hi Joe,

OK - glad it's working for you. It was a 5 minute job and took 5 more minutes to test. :-)

By the way, I did not disable the mode switching code so even though you can't see the mode cycling through the
four modes U / L / + / - it is doing so. This will cause a slight shift in frequency(600 Hz) when you are in either
CW+ or CW- and in RCV mode (Header 7 shorted). U and L will be "right on" in either transmit or receive mode.
Since you are using it as a signal generator and never want the CW offset, you are will always be OK as long as
you don't inadvertently get into CW+ or CW- and also short the two pins of HDR7 indicating RCV mode.

Glad to help you out, Joe.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ag4qc" <ag4qc@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, July 31, 2011 1:20 AM
Subject: [PPLL-VFO] Re: Frequency display - new version 7;7a for AG5QC

> Craig,
> I just loaded the hex code and it works great. I don't even seem to have the +/-/L/U options any more. It looks like I only have
> the 1-4 Menu options, which is great. That and the debug data is also gone. So for my use, it's all good. Man, talk about
> customer service, you are a breath of fresh air!
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> Thank you again,
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> - Joe AG4QC
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> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
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117. Re: Frequency display - new version 7.7a for AG5QC

Yahoo group: PPLL-VFO
Date: 2011-07-31 18:37:20 UTC
From: Jim Dunlap
Topic: 116 Message: 117

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Joe,
>
> OK - glad it's working for you. It was a 5 minute job and took 5 more minutes to test. :-)

It also took five minutes for me to figure out how to modify that code. Plus another five days.

Regards,

Jim D.

118. Mounting the LCD

Yahoo group: PPLL-VFO
Date: 2011-08-01 03:05:35 UTC
From: ag4qc
Topic: 118 Message: 118

I have never been any good at cutting straight lines in metal. So I always end up with a non professional looking cabinet when I have to mount an LCD. But I know some LCD's come with a plastic collar that snaps into the hole and has maybe a 1/8th inch lip that overlaps the edge. It sure makes it look nice. But I can't seem to find a place to just buy the collars. Does anyone have any experience that can help? I was thinking maybe I just need to use the printer and print a nice faceplate on the laser printer and that would cover any imperfections. I guess this is a bit off topic, so feel free ignore it.

73
Joe AG4QC

119. Re: Source code and my reason for pulling it

Yahoo group: PPLL-VFO
Date: 2011-08-01 08:04:48 UTC
From: Andrew Mason
Topic: 82 Message: 119

Hi Craig,
Just a big thank you for your contribution to the amateur community with the code and the quality projects you have developed, and made available to all. Your effort is much appreciated.
73
Andrew
VK4JAM

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi all,
>
> I said I would provide a little more information about my decision to pull the source code for the PEgen570 application from the FILES section of this forum and also from my web page.
>
> I'm not going to go into a lot of detail but I will say that I have been involved in some extended, semi-public conversations with individuals about how I *owe* it to them and the public in general to release all source code for every project that I develop. As many of you know, I have released the complete source code for many different projects and have helped and encouraged many people make changes to the code. I have done so because I wanted to, not because someone told me I *had* to do so. When I am accosted in public by individuals that don't contribute anything and they tell me that it is my *social responsibility*, I start to revolt. Some of these folks have also told me that software patents are *always evil*, and, as the holder of seven of them, I believe that they can have some value in protecting developer's rights for a limited period of time. I am starting to understand why the vast majority of folks NEVER release their source code.
>
> I've been on vacation this past week - enjoying the beauty of Glacier National Park. While there I spent some time reading a couple of seemingly incongruous books, my Bible and a book called "Atlas Shrugged" by the avowed atheist, Ayn Rand. They are far apart in many fundamental ways and I think Ayn Rand misses the fundamental truth about how God is involved in our lives and is even higher in importance than man's deep thinking and reasoning. Nevertheless, they both have some profound, invaluable truths and they both contributed to my thinking along this line.
>
> I will think it over and some day I may decide to post the source code again. We'll see. In the mean time, to those of you that have already downloaded it, please extend to me the courtesy of not re-posting or re-distributing it here or elsewhere.
>
> Respectfully,
> -Craig, AA0ZZ
>
>
> --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:

> >
> > Hi Folks,
> > Yesterday I pulled the file containing the source code for the PEgen570 application from the FILES section of this group and also from my web site. The HEX file for loading the code into a PIC is still there. I will explain more in a couple of days. In the mean time, to those that have already downloaded it, please do me the courtesy of NOT re-posting it. I'll explain shortly.
> > Best Regards,
> > -Craig, AA0ZZ
> >
>

120. Re: Frequency display - new version 7.7a for AG4QC

Yahoo group: PPLL-VFO
Date: 2011-08-01 17:59:58 UTC
From: AA0ZZ
Topic: 116 Message: 120

Oops. Sorry about messing up your call, Joe.
-Craig

121. W6JL User Pages - updated

Yahoo group: PPLL-VFO
Date: 2011-08-05 02:53:16 UTC
From: AA0ZZ
Topic: 121 Message: 121

Hi Folks,

Just to let you know that I've received some new pictures and descriptions of the beautiful homebrewing work that Don, W6JL, has been doing. If you are interested in making a receiver using the Si570 daughtercard and control board with a "Tayloe Mixer" you really should look at this.

The write-up is on my web page under Si570 User Pages.
Direct link: http://cbjohn.com/aa0zz/PPLLUsers/W6JL/W6JL.pdf

It's beautiful work. Thanks, Don!

If anyone else wants to post some info about what you are doing with the Si570, please send me your pictures and writeup! (aa0zz@...) I'd love to add your write-up to the list so others can enjoy it too. I'll make it into a PDF file and post it.

Best Regards,
-Craig, AA0ZZ

122. Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-05 21:09:53 UTC
From: M5FRA - Colin
Topic: 122 Message: 122

This might be a totally stupid question but I am looking for a way of sweeping portions of frequencies, via an external voltage ramp, between say 1 and 30mhz. That could be split into several bands. Is there a way of doing this with a PPLL-VFO? Or do I need to build several conventional VCOs?

Colin - G8FRA/M5FRA

www.m5fra.org.uk

123. Re: W6JL User Pages - updated - again

Yahoo group: PPLL-VFO
Date: 2011-08-06 00:03:16 UTC
From: AA0ZZ
Topic: 121 Message: 123

Hi again,
I forgot to include one of Don's schematics in his write-up. It's a "Lower-Sideband-Only" Tayloe mixer - done this way for simplicity and fewer parts. As Don says, "when you spend all your time on 40 meters CW, who needs USB"? Very interesting, and good to think about.

(See pointer below.)

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi Folks,
>
> Just to let you know that I've received some new pictures and descriptions of the beautiful homebrewing work that Don, W6JL, has been doing. If you are interested in making a receiver using the Si570 daughtercard and control board with a "Tayloe Mixer" you really should look at this.
>
> The write-up is on my web page under Si570 User Pages.
> Direct link: http://cbjohn.com/aa0zz/PPLLUsers/W6JL/W6JL.pdf
>
> It's beautiful work. Thanks, Don!
>
>
> If anyone else wants to post some info about what you are doing with the Si570, please send me your pictures and writeup! (aa0zz@...) I'd love to add your write-up to the list so others can enjoy it too. I'll make it into a PDF file and post it.
>
> Best Regards,
> -Craig, AA0ZZ
>

124. Re: [PPLL-VFO] Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-06 07:10:50 UTC
From: M5FRA - Colin
Topic: 122 Message: 124

I should have explained more, what I want to do is make an HF sweep oscillator for use to testing and aligning filters. I could use a spectrum analyser with a tracking generator but do not have the cash for such a purchase. I found an article in the March 1994 QEX by WI5W and thought about replacing multiple transistor VCOs with a single osc. There is the si571 with its FM input but the frequency swing is not enough, obvious really as it is designed for FM modulation. There are commercial; VCOs available but most have a relatively narrow frequency range, good for VHF bands but not HF. So it looks like it is back to the conventional transistor VCO design.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "M5FRA - Colin" <m5fra@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 05/08/2011 22:09:53
Subject: [PPLL-VFO] Frequency sweeping
>
>
>This might be a totally stupid question but I am looking for a way of
>sweeping portions of frequencies, via an external voltage ramp,
>between say 1 and 30mhz. That could be split into several bands. Is
>there a way of doing this with a PPLL-VFO? Or do I need to build
>several conventional VCOs?
>
>
>Colin - G8FRA/M5FRA
>
>http://www.m5fra.org.uk/
>
>
>
>

125. Re: [PPLL-VFO] Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-06 07:24:01 UTC
From: Stephen Farthing
Topic: 122 Message: 125

Hi Colin,

I am not sure if this will help but G0BBL, Jan Verduyn, sells a USB Si570 synth kit which is controlled from a PC. So it would be possible to write some software that does what you want. Details of the kit are at www.sdr-kits.net. I was the beta tester for the first version of the kit and can assure you that it works. It is widely used in the softrock SDR community and works with a number of the common SDR packages. However the issue for you, I guess, is finding one that does what you need...

73s Steve G0XAR

On 6 August 2011 08:10, M5FRA - Colin <m5fra@...> wrote:

> **
>
>
> I should have explained more, what I want to do is make an HF sweep
> oscillator for use to testing and aligning filters. I could use a spectrum
> analyser with a tracking generator but do not have the cash for such a
> purchase. I found an article in the March 1994 QEX by WI5W and thought about
> replacing multiple transistor VCOs with a single osc. There is the si571
> with its FM input but the frequency swing is not enough, obvious really as
> it is designed for FM modulation. There are commercial; VCOs available but
> most have a relatively narrow frequency range, good for VHF bands but not
> HF. So it looks like it is back to the conventional transistor VCO design.
>
> Colin - G8FRA/M5FRA
>
> www.m5fra.org.uk
>
>
> ------ Original Message ------
> From: "M5FRA - Colin" <m5fra@...>
> To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
> Sent: 05/08/2011 22:09:53
> Subject: [PPLL-VFO] Frequency sweeping
>
>
>
>
> This might be a totally stupid question but I am looking for a way of
> sweeping portions of frequencies, via an external voltage ramp, between say
> 1 and 30mhz. That could be split into several bands. Is there a way of doing
> this with a PPLL-VFO? Or do I need to build several conventional VCOs?
>
>

> Colin - G8FRA/M5FRA
>
> <http://www.m5fra.org.uk>http://www.m5fra.org.uk/
>
>
>
>
>

--
It is vain to do with more that which can be done with less.

126. Re[2]: [PPLL-VFO] Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-06 09:03:08 UTC
From: M5FRA - Colin
Topic: 122 Message: 126

Steve, thanks for the reply. I have one of Jan's kits and am using it
in a multiband transceiver. Unfortunately I cannot do the software bit,
too old and have always been into hardware!

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "Stephen Farthing" <squirrox@gmail.com>
To: PPLL-VFO@yahoogroups.com
Sent: 06/08/2011 08:24:01
Subject: Re: [PPLL-VFO] Frequency sweeping
>
>
>Hi Colin,
>I am not sure if this will help but G0BBL, Jan Verduyn, sells a USB
>Si570 synth kit which is controlled from a PC. So it would be possible
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>packages. However the issue for you, I guess, is finding one that does
>what you need...
>
>73s Steve G0XAR
>
>On 6 August 2011 08:10, M5FRA - Colin <m5fra@...> wrote:
>>
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>>spectrum analyser with a tracking generator but do not have the cash
>>for such a purchase. I found an article in the March 1994 QEX by WI5W
>>and thought about replacing multiple transistor VCOs with a single
>>osc. There is the si571 with its FM input but the frequency swing is
>>not enough, obvious really as it is designed for FM modulation. There
>>are commercial; VCOs available but most have a relatively narrow
>>frequency range, good for VHF bands but not HF. So it looks like it
>>is back to the conventional transistor VCO design.
>>
>>Colin - G8FRA/M5FRA
>>
>>http://www.m5fra.org.uk/
>>
>>
>>------ Original Message ------

>>From: "M5FRA - Colin" <m5fra@...>
>>To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
>>Sent: 05/08/2011 22:09:53
>>Subject: [PPLL-VFO] Frequency sweeping
>>>
>>>
>>>This might be a totally stupid question but I am looking for a way
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>>>
>>>Colin - G8FRA/M5FRA
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>>>http://www.m5fra.org.uk/
>>>
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>>>
>
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>
>--
>It is vain to do with more that which can be done with less.
>
>
>

127. Re: [PPLL-VFO] Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-06 14:11:38 UTC
From: Craig Johnson, AA0ZZ
Topic: 122 Message: 127

Colin,

The difficult issue with using a Si570 for this application is the length of span - no matter what hardware platform for the Si570 you use.
The Si570 ALWAYS requires a freeze/unfreeze operation when the Si570-generated frequency changes more than .35% from the last
freeze/unfreeze. It takes about 10 mS to restart the Si570 after the freeze/unfreeze. This would throw the sweep timing off, of course,
so it would have to be avoided and this means the frequency sweep would have to be very limited - probably too limited. At 10 MHz,
.35% is 35 kHz, at 15 MHz it's 52.5 kHz and at 30 MHz it's 105 kHz. For filter evaluation I assume you will want to sweep a wider
range - probably several MHz - so I would say for this application the Si570 is probably not the best way to go.

A DDS is a natural for this kind of instrument. A couple of years ago (before I started playing with the Si570) I was working on a sweep
generator that worked on a DDS-60 daughtercard in the PIC-EL board. I did a bunch of tricks in that software to make the DDS frequency
changes fast. It takes too long to do the full-blown DDS frequency calculation (one very large multiplication) so I broke the sweep interval
into "steps" (512 steps per sweep, as I recall) and then I would simply add a "DDS step size" parameter to the base DDS parameter to
change the frequency. This made it very fast. The other main requirement of this kind of instrument is some sort of oscilloscope
synchronization (trigger) signal. I generated a pulse at the start of the sweep on an unused PIC pin for this. I had the "guts" of this app
working and was working on the user interface - allowing the operator to specify the upper and lower limits of the sweep - but then I was
swept away to other things and never finished it.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: M5FRA - Colin
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, August 06, 2011 2:10 AM
Subject: Re: [PPLL-VFO] Frequency sweeping

I should have explained more, what I want to do is make an HF sweep oscillator for use to testing and aligning filters. I could use a spectrum analyser with a tracking generator but do not have the cash for such a purchase. I found an article in the March 1994 QEX by WI5W and thought about replacing multiple transistor VCOs with a single osc. There is the si571 with its FM input but the frequency swing is not enough, obvious really as it is designed for FM modulation. There are commercial; VCOs available but most have a relatively narrow

frequency range, good for VHF bands but not HF. So it looks like it is back to the conventional transistor VCO design.

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "M5FRA - Colin" <m5fra@...>
To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
Sent: 05/08/2011 22:09:53
Subject: [PPLL-VFO] Frequency sweeping

This might be a totally stupid question but I am looking for a way of sweeping portions of frequencies, via an external voltage ramp, between say 1 and 30mhz. That could be split into several bands. Is there a way of doing this with a PPLL-VFO? Or do I need to build several conventional VCOs?

Colin - G8FRA/M5FRA

http://www.m5fra.org.uk/

128. Re[2]: [PPLL-VFO] Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-07 05:57:08 UTC
From: M5FRA - Colin
Topic: 122 Message: 128

Craig, thanks for the response. The QEX article was mainly concerned with crystal filters so a wide sweep is not essential. The article also says it need not be fast. I did think about making a sweeper that would also do BPFs and LPFs but that would require a wider sweep. Appreciate the problems with the PPLL-VFO and am thinking of keeping things simple and going back to conventional varicap diode/transistor oscillators. The only problem with that is needing a few to get the frequency range if I want to include L/C filters for HF.

Interesting comments about DDS. This is a time when I really wish I could write the code to do these things!

Colin - G8FRA/M5FRA

www.m5fra.org.uk

------ Original Message ------
From: "Craig Johnson, AA0ZZ" <aa0zz@...>
To: PPLL-VFO@yahoogroups.com
Sent: 06/08/2011 15:11:38
Subject: Re: [PPLL-VFO] Frequency sweeping
>□
>
>Colin,
>
>The difficult issue with using a Si570 for this application is the
>length of span - no matter what hardware platform for the Si570 you
>use.
>The Si570 ALWAYS requires a freeze/unfreeze operation when the
>Si570-generated frequency changes more than .35% from the last
>freeze/unfreeze. It takes about 10 mS to restart the Si570 after the
>freeze/unfreeze. This would throw the sweep timing off, of course,
>so it would have to be avoided and this means the frequency sweep
>would have to be very limited - probably too limited. At 10 MHz,
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>range - probably several MHz - so I would say for this application the
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>(before I started playing with the Si570) I was working on a sweep
>generator that worked on a DDS-60 daughtercard in the PIC-EL board. I
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>changes fast. It takes too long to do the full-blown DDS frequency
>calculation (one very large multiplication) so I broke the sweep

>interval
>into "steps" (512 steps per sweep, as I recall) and then I would
>simply add a "DDS step size" parameter to the base DDS parameter to
>change the frequency. This made it very fast. The other main
>requirement of this kind of instrument is some sort of oscilloscope
>synchronization (trigger) signal. I generated a pulse at the start of
>the sweep on an unused PIC pin for this. I had the "guts" of this app
>working and was working on the user interface - allowing the operator
>to specify the upper and lower limits of the sweep - but then I was
>*swept away* to other things and never finished it.
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>Best Regards,
>-Craig, AA0ZZ
>
>>----- Original Message -----
>>From:M5FRA - Colin
>>To:PPLL-VFO@yahoogroups.com
>>Sent: Saturday, August 06, 2011 2:10 AM
>>Subject: Re: [PPLL-VFO] Frequency sweeping
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>>I should have explained more, what I want to do is make an HF sweep
>>oscillator for use to testing and aligning filters. I could use a
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>>for such a purchase. I found an article in the March 1994 QEX by WI5W
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>>not enough, obvious really as it is designed for FM modulation. There
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>>is back to the conventional transistor VCO design.
>>
>>Colin - G8FRA/M5FRA
>>
>>http://www.m5fra.org.uk/
>>
>>
>>------ Original Message ------
>>From: "M5FRA - Colin" <m5fra@...>
>>To: "PPLL-VFO@yahoogroups.com" <PPLL-VFO@yahoogroups.com>
>>Sent: 05/08/2011 22:09:53
>>Subject: [PPLL-VFO] Frequency sweeping
>>>
>>>
>>>This might be a totally stupid question but I am looking for a way
>>>of sweeping portions of frequencies, via an external voltage ramp,
>>>between say 1 and 30mhz. That could be split into several bands. Is
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>>>
>>>Colin - G8FRA/M5FRA
>>>
>>>http://www.m5fra.org.uk/
>>>
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>>>
>
>
>

129. Re: Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-07 10:06:34 UTC
From: ag4qc
Topic: 122 Message: 129

Wouldn't it make some sense to just set the 570 at one frequency and then sweep it with a mixer and a sweeping oscillator? I guess it depends on how wide of a sweep you are looking to achieve. But with the ability of the 570 being so stable yet flexible, and a mixer, you should be able to make a stable sweeping oscillator to mix.

Joe AG4QC

--- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
>
> Craig, thanks for the response. The QEX article was mainly concerned
> with crystal filters so a wide sweep is not essential. The article also
> says it need not be fast. I did think about making a sweeper that would
> also do BPFs and LPFs but that would require a wider sweep. Appreciate
> the problems with the PPLL-VFO and am thinking of keeping things simple
> and going back to conventional varicap diode/transistor oscillators.
> The only problem with that is needing a few to get the frequency range
> if I want to include L/C filters for HF.
>
> Interesting comments about DDS. This is a time when I really wish I
> could write the code to do these things!
>
> Colin - G8FRA/M5FRA
>
> www.m5fra.org.uk
>

130. Re: [PPLL-VFO] Re: Frequency sweeping

Yahoo group: PPLL-VFO
Date: 2011-08-07 13:27:26 UTC
From: Craig Johnson, AA0ZZ
Topic: 122 Message: 130

Sure, an IF frequency and a mixer would work. This makes it a little more complicated, of course, because it's another element to
control. You want to be able to change the length of the span of the sweep and you want a good trigger signal at the start of the
sweep. Having changeable limits on the sweep frequency is important too, and it's nice to have the limits displayed so you know
where you are.

Yes, to characterize a crystal filter is quite different than characterizing a LPF or BPF, as you say. The Si570 could be ideal
for a crystal filter.

The only real problem I had in making the PIC-EL / DDS-60 sweep generator was the limited number of pushbuttons for the user
interface. With only three or four pushbuttons it was a little tedious to make an easy way for the operator to change the upper
and lower limits. I didn't use the encoder but that would probably be the best way - along with the pushbuttons. For the LPF and
BPF I think the operator will typically want to continually change the sweep limits and to know exactly what the limits are at all
times - to make the best display on the scope for the area in question. The sweep time must be predictable and the steps between
samples (assuming digital) consistent and predictable.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ag4qc" <ag4qc@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, August 07, 2011 5:06 AM
Subject: [PPLL-VFO] Re: Frequency sweeping

> Wouldn't it make some sense to just set the 570 at one frequency and then sweep it with a mixer and a sweeping oscillator? I guess
> it depends on how wide of a sweep you are looking to achieve. But with the ability of the 570 being so stable yet flexible, and a
> mixer, you should be able to make a stable sweeping oscillator to mix.
>
> Joe AG4QC
>
> --- In PPLL-VFO@yahoogroups.com, "M5FRA - Colin" <m5fra@...> wrote:
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>> Craig, thanks for the response. The QEX article was mainly concerned
>> with crystal filters so a wide sweep is not essential. The article also
>> says it need not be fast. I did think about making a sweeper that would

>> also do BPFs and LPFs but that would require a wider sweep. Appreciate
>> the problems with the PPLL-VFO and am thinking of keeping things simple
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>> Colin - G8FRA/M5FRA
>>
>> www.m5fra.org.uk
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> ------------------------------------
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> Yahoo! Groups Links
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>
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131. Source code changes?

Yahoo group: PPLL-VFO
Date: 2011-08-08 04:41:01 UTC
From: ag4qc
Topic: 131 Message: 131

I was wondering if we wanted to have a file section for changes people make in the source code. I can understand it can be confusing when there are a bunch of peoples making changes to the code and either not well tested or the version not changed. I ask because I'm looking at making a simple change that others might find interesting.

As stated in other messages, I am using this as a simple signal generator and it works GREAT!. But because I don't need any other bells and whistles, I was thinking about making a change to the pic code. What I have in mind is the encoder that came with the kit has a N/O push switch function that's not used. I am considering using that inpalcae of sw3. Then I end up with a one knob operation. So I'm considering changing the code so that sw3 will increase the resolution as it normally does. But when it hits the end it would reset back to the beginning so in affect I wouldn't need sw4 at all as it would loop with sw3. This would be really nice and easy. I would still have the calibrate function of sw3 but really, in my use, sw4 would be abandoned.

Anyway, if I do this I was wondering if I should post the changes to the forum. I know we already have a version that has changes made to hide the leading symbol. I'm sort of wondering what the group thinks about the hardware modification and also if we should entertain a bunch of 'hacks' of the code? I know support could be a issue along with opening a can of worms..

73
Joe Ag4QC

132. Re: Source code changes? - New Directory in FILES

Yahoo group: PPLL-VFO
Date: 2011-08-08 12:44:45 UTC
From: AA0ZZ
Topic: 131 Message: 132

Joe,

--- In PPLL-VFO@yahoogroups.com, "ag4qc" <ag4qc@...> wrote:
>
> I was wondering if we wanted to have a file section for changes people make in the source code. I can understand it can be confusing when there are a bunch of peoples making changes to the code and either not well tested or the version not changed. I ask because I'm looking at making a simple change that others might find interesting.

That's a good idea. I have created a new directory in the FILES section called PEgen570 User Mods. Anyone can post code here.
Be sure to include your name/call/Email so folks can contact you if they have questions. Also be sure to provide a good description of your change.

> As stated in other messages, I am using this as a simple signal generator and it works GREAT!. But because I don't need any other bells and whistles, I was thinking about making a change to the pic code. What I have in mind is the encoder that came with the kit has a N/O push switch function that's not used. I am considering using that inpalcae of sw3. Then I end up with a one knob operation. So I'm considering changing the code so that sw3 will increase the resolution as it normally does. But when it hits the end it would reset back to the beginning so in affect I wouldn't need sw4 at all as it would loop with sw3. This would be really nice and easy. I would still have the calibrate function of sw3 but really, in my use, sw4 would be abandoned.
>
Sounds like a good idea for you app, Joe. I didn't use the pushbutton of the encoder becaue the I wanted to make it compatible with the PIC-EL and I don't have the contacts for the shaft pushbutton switch wired to PIC pins in the PIC-EL. The PIC-EL has the footprint and hole layout two different encoders - the larger encoder with the shaft switch (the encoder that we use in the Si570 control board kit) and also the standard, mechanical encoder that does not have the shaft pushbutton switch. Rewiring the control board to use the shaft pushbutton sounds like a good idea for folks that are willing to add some wires.

> Anyway, if I do this I was wondering if I should post the changes to the forum. I know we already have a version that has changes made to hide the leading symbol. I'm sort of wondering what the group thinks about the hardware modification and also if we should entertain a bunch of 'hacks' of the code? I know support could be a issue along with opening a can of worms..
> 73
> Joe Ag4QC
>
Please do. Nothing like a good can of worms for breakfast. :-) Seriously, it will be good to see what you all come up with.

Best Regards,
-Craig, AA0ZZ

133. Pop

Yahoo group: PPLL-VFO
Date: 2011-08-09 00:04:37 UTC
From: Jim Dunlap
Topic: 133 Message: 133

Just finished with a home brew version with a 1x8 lcd. Controller works great with the 570 chip. I'm still getting the "pop" when crossing the 3.5% limit. Of course, it is running open with no shielding on the bench, at present. Is the "pop" supposed to be suppressed completely? It is fairly loud and a little annoying. On 40 meters, it occurs about every 24 kc. The version notes v7.4 say, "Remove setting of NEW FREQ bit during UNFREEZE-M. No pops in speaker now." I'm using v7.6 software. Have I missed something?

Jim D.

134. Re: [PPLL-VFO] Pop

Yahoo group: PPLL-VFO
Date: 2011-08-09 02:00:12 UTC
From: Craig Johnson, AA0ZZ
Topic: 133 Message: 134

Jim,

There are two kinds of FREEZEs, the "standard" FREEZE and the FREEZE-M. The Si570 requires that you to use the "standard" FREEZE / UNFREEZE every time you change the frequency by more than .35% since the last FREEZE / UNFREEZE. That's the pop you hear, and I don't think there is anything that can be done about it (other than audio filtering - more later). Yes, you can probably "push it" a little bit but that's what the spec sheet says. It's sort of like driving the Si570 below 10 MHz. Yes, it can be done to some extent but it is not guaranteed by Silicon Labs.) The PLL simply must be stopped and restarted. In my QEX article (posted on my web page) I show an oscilloscope trace of the 10 ms drop-out which occurs after the Si570 starts up again after an unfreeze.

The FREEZE-M is a different animal and a FREEZE-M / UNFREEZE sequence doesn't cause the pop because it doesn't really cause the PLL to stop. Using the FREEZE-M / UNFREEZE does NOT replace the requirement for the "standard" FREEZE/UNFREEZE sequence afret .35% change. The FREEZE-M is simply used to keep the Si570 from spraying all over unknown frequencies as the Si570 parameters are being loaded. The original version of the Si570 that I was playing with did not have the FREEZE-M and I really worried about this. They added the FREEZE-M to the Si598 first, and I nearly switched over to that chip simply to get this feature. Then one day I was Emailing with a Silicon Labs technical support guy and he told me that the Si570 also had the FREEZE-M function added but just wasn't documented in the spec sheet yet. The Si570 has some significant performance improvements over the Si598 so I switched back.

I had several iterations of the code as I was figuring out how the FREEZE / UNFREEZE and FREEZE-M / UNFREEZE works. For a while I thought a NEW FREQ was required after the FREEZE-M, just as it is after the "standard" FREEZE; however it is not. If the NEW FREQ bit is set, the pop will occur, so I now do not set the NEW FREQ bit after a FREEZE-M. The NEW FREQ bit still must be set after the "standard" FREEZE / UNFREEZE operation; hence the pop.

That being said, I don't know of any change in the FREEZE functionality between 7.4 and 7.6. Please confirm this. Of course, if you hear the pop as you pass a particular frequency, you will not continue to hear it every time you pass back and forth on that frequency because that frequency will now be the new "center frequency". I'm sure you understand this but I'm just trying to clarify it for everyone. The statement in the comments at the beginning of the source code

that says "Remove setting of NEW FREQ
bit during UNFREEZE-M. No pops in speaker now." was implemented in version 7.4 and was not changed in v7.5 or v7.6.

I have considered adding some sort of audio filtering circuitry to filter out the pop but I didn't think it occurred often enough to
be that annoying. I was going to engage the audio filter before issuing the standard FREEZE and then disengaging it after the
UNFREEZE. Maybe this should be reconsidered.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "Jim Dunlap" <roz5bw@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, August 08, 2011 7:04 PM
Subject: [PPLL-VFO] Pop

> Just finished with a home brew version with a 1x8 lcd. Controller works great with the 570 chip. I'm still getting the "pop"
> when crossing the 3.5% limit. Of course, it is running open with no shielding on the bench, at present. Is the "pop" supposed to
> be suppressed completely? It is fairly loud and a little annoying. On 40 meters, it occurs about every 24 kc. The version notes
> v7.4 say, "Remove setting of NEW FREQ bit during UNFREEZE-M. No pops in speaker now." I'm using v7.6 software. Have I missed
> something?
>
> Jim D.
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> Yahoo! Groups Links
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135. Re: Pop - A little more

Yahoo group: PPLL-VFO
Date: 2011-08-09 12:51:37 UTC
From: AA0ZZ
Topic: 133 Message: 135

Hi again,
A few more thoughts about audio filtering.

By the way, in the previous message I should have called the "standard" FREEZE the FREEZE DCO as I do in the QEX article. That's a better name.

If you look at Figure 3 in the article (click on the QEX cover to open the article in PDF format) you will see the oscilloscope traces that show this RF dropout and the resulting audio pop. The time scales of the two traces (3a and 3b) are different so be careful. The time scales are labelled in the pictures. You will see that the audio "pop" (figure 3b) occurs after the unfreeze. Note that the RF dropout is not the full 10ms here (not sure when it does take the full 10ms) but it's only about 220us here. The audio pop (increased amplitude)starts right at the end of the DCO unfreeze and hits its peak about 1 ms later. It's all over in about 4 mS.

I haven't thought too much about how to remove this pop but my initial thought was to mute the receiver (using a FET) for a few milliseconds (maybe 4 ms - a few audio cycles) after the unfreeze. I'm not sure how noticeable this muting action would be. Perhaps it would be more annoying than the pop.

Need some experimenters to think about this and see if we can come up with something.

Best Regards,
-Craig, AA0ZZ

138. Building the Controller

Yahoo group: PPLL-VFO
Date: 2011-09-07 13:50:05 UTC
From: Fernando Krouwel
Topic: 138 Message: 138

Hi Craig, good morning:

Thank you very much for the approval.

Since some time ago, I have been fighting with an experimental AVR based Si570 controller to use in conjunction with a ready populated (and already working) WB6DHW Si570 support board (it converts 5V I2C lines into 3.3V I2C for the Si570 and also has a voltage regulator to power the Si570 with 3.3V starting from 5V or 12V, which can be used as a daughtercard to your controller.

So, I have in hands the most important materials, including a never used 16F88 PIC, in my new components box.

Some of these days I will start building it, possibly in a standard ready made PCB.
Is it possible to purchase only the naked (unpopulated) PCB for building the controller?

73?s
Fernando - PY2ETT

----- Original Message -----
From: "PPLL-VFO Moderator" <PPLL-VFO-owner@yahoogroups.com>
To: <flky661@...>
Sent: Tuesday, September 06, 2011 10:02 PM
Subject: Yahoo! Groups: Welcome to PPLL-VFO. Visit today!

>
> Welcome to the PPLL-VFO group at Yahoo! Groups.
>
> Best Regards,
> Craig, AA0ZZ,
> Moderator, PPLL-VFO
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> Your use of Yahoo! Groups is subject to http://docs.yahoo.com/info/terms/
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No virus found in this incoming message.
Checked by AVG - www.avg.com
Version: 8.5.449 / Virus Database: 271.1.1/3880 - Release Date: 09/06/11
06:35:00

139. Re: Building the Controller

Yahoo group: PPLL-VFO
Date: 2011-09-07 15:37:55 UTC
From: AA0ZZ
Topic: 138 Message: 139

Hi Fernando,

Yes, you can get the bare board from Bill Kelsey, N8ET, at Kanga.
http://kangaus.com/si570_project.htm

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "Fernando Krouwel" <flky661@...> wrote:
>
> Hi Craig, good morning:
>
> Thank you very much for the approval.
>
> Since some time ago, I have been fighting with an experimental AVR based
> Si570 controller to use in conjunction with a ready populated (and already
> working) WB6DHW Si570 support board (it converts 5V I2C lines into 3.3V I2C
> for the Si570 and also has a voltage regulator to power the Si570 with 3.3V
> starting from 5V or 12V, which can be used as a daughtercard to your
> controller.
>
> So, I have in hands the most important materials, including a never used
> 16F88 PIC, in my new components box.
>
> Some of these days I will start building it, possibly in a standard ready
> made PCB.
> Is it possible to purchase only the naked (unpopulated) PCB for building the
> controller?
>
> 73´s
> Fernando - PY2ETT
>
>
> ----- Original Message -----
> From: "PPLL-VFO Moderator" <PPLL-VFO-owner@yahoogroups.com>
> To: <flky661@...>
> Sent: Tuesday, September 06, 2011 10:02 PM
> Subject: Yahoo! Groups: Welcome to PPLL-VFO. Visit today!
>
>
> >
> > Welcome to the PPLL-VFO group at Yahoo! Groups.
> >
> > Best Regards,
> > Craig, AA0ZZ,
> > Moderator, PPLL-VFO

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> > Your use of Yahoo! Groups is subject to http://docs.yahoo.com/info/terms/
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> No virus found in this incoming message.
> Checked by AVG - www.avg.com
> Version: 8.5.449 / Virus Database: 271.1.1/3880 - Release Date: 09/06/11
> 06:35:00
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140. Re: [PPLL-VFO] Re: Building the Controller

Yahoo group: PPLL-VFO
Date: 2011-09-07 22:35:24 UTC
From: Dale
Topic: 138 Message: 140

AA0ZZ <aa0zz@cbjohn.com> wrote:

>Hi Fernando,
>
>Yes, you can get the bare board from Bill Kelsey, N8ET, at Kanga.
>http://kangaus.com/si570_project.htm
>
>Best Regards,
>-Craig, AA0ZZ
>
>
>--- In PPLL-VFO@yahoogroups.com, "Fernando Krouwel" <flky661@...> wrote:
>>
>> Hi Craig, good morning:
>>
>> Thank you very much for the approval.
>>
>> Since some time ago, I have been fighting with an experimental AVR based
>> Si570 controller to use in conjunction with a ready populated (and already
>> working) WB6DHW Si570 support board (it converts 5V I2C lines into 3.3V I2C
>> for the Si570 and also has a voltage regulator to power the Si570 with 3.3V
>> starting from 5V or 12V, which can be used as a daughtercard to your
>> controller.
>>
>> So, I have in hands the most important materials, including a never used
>> 16F88 PIC, in my new components box.
>>
>> Some of these days I will start building it, possibly in a standard ready
>> made PCB.
>> Is it possible to purchase only the naked (unpopulated) PCB for building the
>> controller?
>>
>> 73´s
>> Fernando - PY2ETT
>>
>>
>> ----- Original Message -----
>> From: "PPLL-VFO Moderator" <PPLL-VFO-owner@yahoogroups.com>
>> To: <flky661@...>
>> Sent: Tuesday, September 06, 2011 10:02 PM
>> Subject: Yahoo! Groups: Welcome to PPLL-VFO. Visit today!
>>
>>
>> >
>> > Welcome to the PPLL-VFO group at Yahoo! Groups.

>> >
>> > Best Regards,
>> > Craig, AA0ZZ,
>> > Moderator, PPLL-VFO
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>> > Your use of Yahoo! Groups is subject to http://docs.yahoo.com/info/terms/
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>> No virus found in this incoming message.
>> Checked by AVG - www.avg.com
>> Version: 8.5.449 / Virus Database: 271.1.1/3880 - Release Date: 09/06/11
>> 06:35:00
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>

141. Hi, New here,

Yahoo group: PPLL-VFO
Date: 2011-09-08 02:07:49 UTC
From: kb5zxm
Topic: 141 Message: 141

Thanks for allowing me access to your discussion. And Please excuse my ignorance about PIC programming, I am reading on that now.
My main need for this device, is to replace various oscillators in older equipment. Some of my need involves older test equipment, so ' Freq stability' is a concern. My first project will be to replace a bank of crystals in a radio service monitor made by Cushman. [CE7 and MCM 5]
The cavity where I will install the dds vfo is temp controlled, and and well shielded <from external RF > it, also
houses a 10 Mc crystal, that must remain .
Getting/extending the dds vfo controls and read out display involves a distance of about 15 inches and is well shielded.
The freq range I require for the vfo to cover is from 3Mc to 9.8 Mc , with as much fine tune control as I can get. <<for example 7.087,500 Mc> some of the higher freq's derived from this vfo are in the 1Gc range. Sine wave out put is desired.As it will/must drive a Variable Harmonic amp.
Much later <for use in a Cushman CE6A> I will want build a dds vfo with 10 selectable frequencies and a multiplier[s] to get an output of 1300 to 2200 Mc. to replace a <no longer available> component circuit that feeds a phased lock loop, and will want to give that loop the ability to drift the dds vfo.
My primary query is how to obtain freq stability ? IS it done by going higher in freq,on the clock/primary crystal freq or down?

Much later I would want to up grade my Old Hallicrafters tube trans, and receiver
Well that covers the next decade, But I am not shooting for the moon, the Chinese, and Indians' will be doin that?

142. Re: Hi, New here,

Yahoo group: PPLL-VFO
Date: 2011-09-17 01:01:08 UTC
From: AA0ZZ
Topic: 141 Message: 142

Hi,

--- In PPLL-VFO@yahoogroups.com, "kb5zxm" <kb5zxm@...> wrote:
>
> Thanks for allowing me access to your discussion. And Please excuse my ignorance about PIC programming, I am reading on that now.
> My main need for this device, is to replace various oscillators in older equipment. Some of my need involves older test equipment, so ' Freq stability' is a concern. My first project will be to replace a bank of crystals in a radio service monitor made by Cushman. [CE7 and MCM 5]
> The cavity where I will install the dds vfo is temp controlled, and and well shielded <from external RF > it, also
> houses a 10 Mc crystal, that must remain .
> Getting/extending the dds vfo controls and read out display involves a distance of about 15 inches and is well shielded.
> The freq range I require for the vfo to cover is from 3Mc to 9.8 Mc , with as much fine tune control as I can get. <<for example 7.087,500 Mc> some of the higher freq's derived from this vfo are in the 1Gc range. Sine wave out put is desired.As it will/must drive a Variable Harmonic amp.
> Much later <for use in a Cushman CE6A> I will want build a dds vfo with 10 selectable frequencies and a multiplier[s] to get an output of 1300 to 2200 Mc. to replace a <no longer available> component circuit that feeds a phased lock loop, and will want to give that loop the ability to drift the dds vfo.
> My primary query is how to obtain freq stability ? IS it done by going higher in freq,on the clock/primary crystal freq or down?
>
> Much later I would want to up grade my Old Hallicrafters tube trans, and receiver
> Well that covers the next decade, But I am not shooting for the moon, the Chinese, and Indians' will be doin that?
>
There is no reason why the Si570 device could not be used for your application, giving you a nice, stable frequency source. The problem is going to be the software. My Si570 app is for continuous tuning, not for single, set frequencies or small frequency ranges. The "building block" software is there for you to use as an example but you would have to develop the code.

Best Regards,
-Craig, AA0ZZ

143. Re: Hi, New here,

Yahoo group: PPLL-VFO
Date: 2011-09-17 08:06:12 UTC
From: Stephen Farthing
Topic: 141 Message: 143

Hi,

You should look at the Si570 synth kits produced by www.sdr-kits.net . The PA0KLT kit is designed for continuous frequency tuning.. However it does have button select memories so you can store your spot frequencies and select them. They also offer a USB connectable kit that uses software in a PC to select a spot frequency.

They use AVR 8 Bit processors rather than PICs mostly because there is a free programming system (AVR Studio and GCC). When they started out I don't think this was available for the Microchip PIC chips.

73s Steve G0XAR , from a cold and wet England

--
It is vain to do with more that which can be done with less.

144. Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-17 15:07:50 UTC
From: Richard
Topic: 144 Message: 144

Hi
Has anyone written any s/w just to load a single frequency into a
Si570/1.
There's plenty of choice for using one as a VFO, but all I want is just
to load its o/p frequency on power up. Its a Si571 I have and I want to
use it as a FM modulator.
It would be a useful script as its now a lower cost to buy a Si570
instead of getting a crystal made, something that can run on a small
PIC so as it boots up it loads the Si570/1 and then goes to sleep, until
the next power cycle.
TIA
--
Best wishes / 73
Richard Bown

E-mail: richard@...

nil carborundum a illegitemis
##
Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

145. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-17 18:03:40 UTC
From: Craig Johnson, AA0ZZ
Topic: 144 Message: 145

Hi Richard,

The Si570 board with the Si570 app will do it. All you have to do is tune it to your desired
frequency and then hold down pushbutton 3 for more than 2 seconds. This will save that frequency in EEPROM and it will be used as the start-up frequency from then on.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "Richard" <richard@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Saturday, September 17, 2011 10:07 AM
Subject: [PPLL-VFO] Single frequency loading on Si571

> Hi
> Has anyone written any s/w just to load a single frequency into a
> Si570/1.
> There's plenty of choice for using one as a VFO, but all I want is just
> to load its o/p frequency on power up. Its a Si571 I have and I want to
> use it as a FM modulator.
> It would be a useful script as its now a lower cost to buy a Si570
> instead of getting a crystal made, something that can run on a small
> PIC so as it boots up it loads the Si570/1 and then goes to sleep, until
> the next power cycle.
> TIA
> --
> Best wishes / 73
> Richard Bown
>
> E-mail: richard@...
>
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> Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
> Ham Call:G8JVM
> Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
> QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
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> Yahoo! Groups Links

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146. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-17 22:47:25 UTC
From: Richard
Topic: 144 Message: 146

On Sat, 2011-09-17 at 13:03 -0500, Craig Johnson, AA0ZZ wrote:
> Hi Richard,
>
> The Si570 board with the Si570 app will do it. All you have to do is tune it to your
desired
> frequency and then hold down pushbutton 3 for more than 2 seconds. This will save that
> frequency in EEPROM and it will be used as the start-up frequency from then on.
>
> Best Regards,
> -Craig, AA0ZZ

Hi Craig
just a problem with that, and that is it needs to have attached a
display, buttons and shaft encoder. So I can put the Si571, PIC and
pre-emphasis network, and an RF buffer all on a small pcb less than 2"
square.
Ideally with the wanted frequency directly in the code, entered as a
variable. And if a frequency change was needed, that could be done with
a ICSP connection.
ie
the PIC would already from it programming have the wanted frequency in
the code.

I hope that helps clarify things

--
Best wishes / 73
Richard Bown

E-mail: richard@...

nil carborundum a illegitemis
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Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

147. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 00:42:40 UTC
From: kevin asato
Topic: 144 Message: 147

Not having studied the software completely, but it seems to me that modifying the fields below should at least give you a correct starting frequency:

```
; Default start-up frequency Fout = 10,000,000 for this part
DEFAULTSI570FREQ3 equ 0x00            ; MSB
DEFAULTSI570FREQ2 equ 0x98            ;
DEFAULTSI570FREQ1 equ 0x96            ;
DEFAULTSI570FREQ0 equ 0x80            ; LSB
```

I have not gone through the software far enough to determine the conversion factor back and forth to decimal nor have I seen where omitting the peripherals should cause problems. If in doubt you should be able to stub the non essential I/Os from the code and reassemble. A quick trip through the PIC burner and you should be able to verify things. You can also define a space in RAM space for a second location in which a new value can be loaded at run time. A simple push button discrete can be used to cycle through the additional locations.

It's been years since writing microcontroller code - used to write a lot of assembly language for 8051s, 8088s, 6800s, and 6809s so I'm a bit behind on things. However, this is what I used to do for similar situations. Back then, too, the ICE was my friend which allowed me to patch code on the fly!

73,
kevin
kc6pob

Hi Craig
just a problem with that, and that is it needs to have attached a display, buttons and shaft encoder. So I can put the Si571, PIC and pre-emphasis network, and an RF buffer all on a small pcb less than 2" square.
Ideally with the wanted frequency directly in the code, entered as a variable. And if a frequency change was needed, that could be done with a ICSP connection.
ie
the PIC would already from it programming have the wanted frequency in the code.

I hope that helps clarify things

--
Best wishes / 73
Richard Bown

E-mail: richard@...

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Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

Yahoo! Groups Links

    http://docs.yahoo.com/info/terms/

148. Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 01:20:56 UTC
From: AA0ZZ
Topic: 144 Message: 148

Kevin and group,

--- In PPLL-VFO@yahoogroups.com, kevin asato <kc6pob@...> wrote:
>
> Not having studied the software completely, but it seems to me that modifying the fields below should at least give you a correct starting frequency:
>
> ; Default start-up frequency Fout = 10,000,000 for this part
> DEFAULTSI570FREQ3 equ 0x00   ; MSB
> DEFAULTSI570FREQ2 equ 0x98   ;
> DEFAULTSI570FREQ1 equ 0x96   ;
> DEFAULTSI570FREQ0 equ 0x80   ; LSB
>
> I have not gone through the software far enough to determine the conversion factor back and forth to decimal nor have I seen where omitting the peripherals should cause problems. If in doubt you should be able to stub the non essential I/Os from the code and reassemble. A quick trip through the PIC burner and you should be able to verify things. You can also define a space in RAM space for a second location in which a new value can be loaded at run time. A simple push button discrete can be used to cycle through the additional locations.
>
> It's been years since writing microcontroller code - used to write a lot of assembly language for 8051s, 8088s, 6800s, and 6809s so I'm a bit behind on things. However, this is what I used to do for similar situations. Back then, too, the ICE was my friend which allowed me to patch code on the fly!
>
> 73,
> kevin
> kc6pob
>

No, this is not the place to change it. Those 10 MHz values are there because 10 MHz is the default values of the particular Si570 part number that I am using for the Daughtercard kits. Because of the part number, Silicon Labs sets up the internal parameters of the Si570s to start up at 10 MHz - even without sending any parameters via the I2C communications. These DEFINE values are used in my calibration routine to "work backwards" after I retrieve the default parameters from the Si570. I then am able to determine the exact, calibrated crystal frequency the invididual part that is curently executing. Each Si570 is calibrated by Silicon Labs so the stored parameters will be different for each part. Once the calculation routine is executed and the exact crystal frequency (114,285 MHz nominal) is determined for the part, this crystal frequency is stored in RAM and EEPROM and is used in all subsequent frequency calculations. Pretty neat, huh?

If you want to change the start-up frequency, you can do it the way I previously described (tune to the frequency and hold down pushbutton 3 for 2 seconds to store it in EEPROM). Else, if you really want to change the code you can find the parameter bytes that currently specify the start-up frequency of 14,025,000 in EEPROM and change the bytes there. Holding

pushbutton 3 changes these exact same EEPROM locations.

Best Regards,
-Craig, AA0ZZ

149. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 08:40:36 UTC
From: Francis DUPONT
Topic: 144 Message: 149

Hi Richard, Craig and All,

< Has anyone written any s/w just to load a single frequency
< into a Si570/1?

If you already have the AA0ZZ Si570 Daughtercard and Control Board,
then it is easy and Craig gave the solution.

But if you start from scratch, I think there is a very simple and cheap
way to do this.

Using an ATtiny45 (or better 85) 8 pin device from Atmel, with the PE0FKO
firmware, all you need (if you have the Si570 and its 3V3 regulator) is:

- one USB connector (for the PC side)

- 5 R and 2 C

- 2 x 3V6 zener diodes

- one 3 pin connector to connect to the I2C bus on the Si570 side.

All of these components can be wired on a very small piece of Veroboard.

Using another PE0FKO software on the PC, you can choose "your frequency",
then the Si570 will always be loaded with this frequency on restart.

Of course the PC and the USB cable are only needed for the first operation,
after that the small board with the ATtiny85 works alone as far as you
power the chip with +5V.

This software gives you another very useful tool. You can calibrate your
Si570, if you want an exact frequency. This calibration, like your
starting frequency is stored in EEPROM until next power up.

You can find it here:

< http://home.ict.nl/~fredkrom/pe0fko/CFGSR/ >

You can get an ATtiny85 programmed with the PE0FKO firmware from K5NWA:

<http://thepartsplace.k5nwa.com/index.php?route=product/product&path=39_43&product_id=53>

something like $2.60.

I told you that it was cheap...

Have fun with the Si570.

Best Regards,

Francis

150. Re: [PPLL-VFO] Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 09:03:32 UTC
From: Richard-G8JVM
Topic: 144 Message: 150

On Sun, 2011-09-18 at 01:20 +0000, AA0ZZ wrote:
>
> Kevin and group,
>
> --- In PPLL-VFO@yahoogroups.com, kevin asato <kc6pob@...> wrote:
> >
> > Not having studied the software completely, but it seems to me that
> modifying the fields below should at least give you a correct starting
> frequency:
> >
> > ; Default start-up frequency Fout = 10,000,000 for this part
> > DEFAULTSI570FREQ3 equ 0x00 ; MSB
> > DEFAULTSI570FREQ2 equ 0x98 ;
> > DEFAULTSI570FREQ1 equ 0x96 ;
> > DEFAULTSI570FREQ0 equ 0x80 ; LSB
> >
> > I have not gone through the software far enough to determine the
> conversion factor back and forth to decimal nor have I seen where
> omitting the peripherals should cause problems. If in doubt you should
> be able to stub the non essential I/Os from the code and reassemble. A
> quick trip through the PIC burner and you should be able to verify
> things. You can also define a space in RAM space for a second location
> in which a new value can be loaded at run time. A simple push button
> discrete can be used to cycle through the additional locations.
> >
> > It's been years since writing microcontroller code - used to write a
> lot of assembly language for 8051s, 8088s, 6800s, and 6809s so I'm a
> bit behind on things. However, this is what I used to do for similar
> situations. Back then, too, the ICE was my friend which allowed me to
> patch code on the fly!
> >
> > 73,
> > kevin
> > kc6pob
> >
> No, this is not the place to change it. Those 10 MHz values are there
> because 10 MHz is the default values of the particular Si570 part
> number that I am using for the Daughtercard kits. Because of the part
> number, Silicon Labs sets up the internal parameters of the Si570s to
> start up at 10 MHz - even without sending any parameters via the I2C
> communications. These DEFINE values are used in my calibration routine
> to "work backwards" after I retrieve the default parameters from the
> Si570. I then am able to determine the exact, calibrated crystal
> frequency the invididual part that is curently executing. Each Si570
> is calibrated by Silicon Labs so the stored parameters will be

> different for each part. Once the calculation routine is executed and
> the exact crystal frequency (114,285 MHz nominal) is determined for
> the part, this crystal frequency is stored in RAM and EEPROM and is
> used in all subsequent frequency calculations. Pretty neat, huh?
>
> If you want to change the start-up frequency, you can do it the way I
> previously described (tune to the frequency and hold down pushbutton 3
> for 2 seconds to store it in EEPROM). Else, if you really want to
> change the code you can find the parameter bytes that currently
> specify the start-up frequency of 14,025,000 in EEPROM and change the
> bytes there. Holding pushbutton 3 changes these exact same EEPROM
> locations.
>
> Best Regards,
> -Craig, AA0ZZ

As the default frequency on my Si571 s is 125 MHz, would I need to change the 10 MHz to 125 MHz there, and change the 14.025 MHz to 10.700 MHz, how much of the code can I throw away, I don't need any of the hardware used with it, just pic and Si571.
If the lower limit was made 9.000 MHz, what are the chances of getting on that frequency ?

151. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 09:21:53 UTC
From: Richard
Topic: 144 Message: 151

On Sun, 2011-09-18 at 10:40 +0200, Francis DUPONT wrote:
>
> Hi Richard, Craig and All,
>
> < Has anyone written any s/w just to load a single frequency
> < into a Si570/1?
>
> If you already have the AA0ZZ Si570 Daughtercard and Control Board,
> then it is easy and Craig gave the solution.
>
> But if you start from scratch, I think there is a very simple and
> cheap
> way to do this.
>
> Using an ATtiny45 (or better 85) 8 pin device from Atmel, with the
> PE0FKO
> firmware, all you need (if you have the Si570 and its 3V3 regulator)
> is:
>
> - one USB connector (for the PC side)
>
> - 5 R and 2 C
>
> - 2 x 3V6 zener diodes
>
> - one 3 pin connector to connect to the I2C bus on the Si570 side.
>
> All of these components can be wired on a very small piece of
> Veroboard.
>
> Using another PE0FKO software on the PC, you can choose "your
> frequency",
> then the Si570 will always be loaded with this frequency on restart.
>
> Of course the PC and the USB cable are only needed for the first
> operation,
> after that the small board with the ATtiny85 works alone as far as
> you
> power the chip with +5V.
>
> This software gives you another very useful tool. You can calibrate
> your
> Si570, if you want an exact frequency. This calibration, like your
> starting frequency is stored in EEPROM until next power up.
>

> You can find it here:
>
> < http://home.ict.nl/~fredkrom/pe0fko/CFGSR/ >
>
>
> You can get an ATtiny85 programmed with the PE0FKO firmware from
> K5NWA:
>
>
<http://thepartsplace.k5nwa.com/index.php?route=product/product&path=39_43&product_id=53>
>
> something like $2.60.
>
> I told you that it was cheap...
>
> Have fun with the Si570.
>
>
> Best Regards,
>
> Francis
>
Hi Francis

That sounds better,
Do you know if the startup frequency can be put in the ATMEL device.
I only need one 10.&00 MHz and dont want to have to connect to the
computer via USB to set the frequency.
Maybe try and get an answer out of PE0FKP .

Many thanks for the info

--
Best wishes / 73
Richard Bown

E-mail: richard@...

nil carborundum a illegitemis
##
Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

152. Re: [PPLL-VFO] Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 13:26:12 UTC
From: Craig Johnson, AA0ZZ
Topic: 144 Message: 152

Richard,

> As the default frequency on my Si571 s is 125 MHz, would I need to
> change the 10 MHz to 125 MHz there,

I think this will work. I haven't checked the math on that frequency to see if any of the registers overflow but it should work. You will have to set up the parameters for that frequency.

>and change the 14.025 MHz to 10.700 MHz,

OK.

>how much of the code can I throw away, I don't need any of the
> hardware used with it, just pic and Si571.

Quite a bit. You can throw away all of the tuning (encoder) code and all of the band-switching code, LCD code. the code that checks the frequency span to see if a DCO restart is needed.

> If the lower limit was made 9.000 MHz, what are the chances of getting
> on that frequency ?

Pretty good. Many people have pushed them much lower than that. It's just not guaranteed in the spec and it may differ from one Si571 sample to another. I assume Silicon Labs had a pretty good reason for specifying the lower limit as 10 MHz.

By the way, I assume that the reason why you want to use a Si571 rather than a Si570 is because you already have one sample part. That's fine. For this application there really isn't any advantage in being able to "pull" the frequency by applying a voltage to the VCXO pin so the Si571 (VCXO) really isn't an advantage over the Si570 (XO).. (The voltage-control pin is not connected in the Si570.) The VCXO voltage will affect the calibration and you will have to add some additional circuitry to manually vary that voltage to calibrate the frequency. In the Si570 the calibration can all be done in software.

Best Regards,
-Craig, AA0ZZ

153. Re: [PPLL-VFO] Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 16:13:52 UTC
From: Richard
Topic: 144 Message: 153

On Sun, 2011-09-18 at 08:26 -0500, Craig Johnson, AA0ZZ wrote:
> Richard,
>
> > As the default frequency on my Si571 s is 125 MHz, would I need to
> > change the 10 MHz to 125 MHz there,
>
> I think this will work. I haven't checked the math on that frequency to see if any of
> the registers overflow but it should work. You will have to set up the parameters
> for that frequency.
>
> >and change the 14.025 MHz to 10.700 MHz,
>
> OK.
>
> >how much of the code can I throw away, I don't need any of the
> > hardware used with it, just pic and Si571.
>
> Quite a bit. You can throw away all of the tuning (encoder) code and all of the
> band-switching code, LCD code. the code that checks the frequency span to
> see if a DCO restart is needed.
>
> > If the lower limit was made 9.000 MHz, what are the chances of getting
> > on that frequency ?
>
> Pretty good. Many people have pushed them much lower than that. It's just not
> guaranteed in the spec and it may differ from one Si571 sample to another.
> I assume Silicon Labs had a pretty good reason for specifying the lower limit as
> 10 MHz.
>
> By the way, I assume that the reason why you want to use a Si571 rather than
> a Si570 is because you already have one sample part. That's fine. For this
> application there really isn't any advantage in being able to "pull" the frequency
> by applying a voltage to the VCXO pin so the Si571 (VCXO) really isn't an
> advantage over the Si570 (XO).. (The voltage-control pin is not connected in
> the Si570.) The VCXO voltage will affect the calibration and you will have to
> add some additional circuitry to manually vary that voltage to calibrate the
> frequency. In the Si570 the calibration can all be done in software.
>
> Best Regards,
> -Craig, AA0ZZ
>
>

Thanks Craig,
The reason for the use of the Si571 is I want to use it as an FM

modulator.
Generating FM at 9 MHz is not easy, the range becomes limited by the
varicap diode characteristics which limits the modulation freq.
The Si571 doesn't gave those problems, and should be very linear .
>

--
Best wishes / 73
Richard Bown

E-mail: richard@...

nil carborundum a illegitemis
##
Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

154. Re: [PPLL-VFO] Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 16:32:52 UTC
From: Craig Johnson, AA0ZZ
Topic: 144 Message: 154

Richard,
Ah, that's interesting. Let us know how it goes.
Best Regards,
-Craig

----- Original Message -----
From: "Richard" <richard@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, September 18, 2011 11:13 AM
Subject: Re: [PPLL-VFO] Re: Single frequency loading on Si571

> On Sun, 2011-09-18 at 08:26 -0500, Craig Johnson, AA0ZZ wrote:
>> Richard,
>>
>> > As the default frequency on my Si571 s is 125 MHz, would I need to
>> > change the 10 MHz to 125 MHz there,
>>
>> I think this will work. I haven't checked the math on that frequency to see if any of
>> the registers overflow but it should work. You will have to set up the parameters
>> for that frequency.
>>
>> >and change the 14.025 MHz to 10.700 MHz,
>>
>> OK.
>>
>> >how much of the code can I throw away, I don't need any of the
>> > hardware used with it, just pic and Si571.
>>
>> Quite a bit. You can throw away all of the tuning (encoder) code and all of the
>> band-switching code, LCD code. the code that checks the frequency span to
>> see if a DCO restart is needed.
>>
>> > If the lower limit was made 9.000 MHz, what are the chances of getting
>> > on that frequency ?
>>
>> Pretty good. Many people have pushed them much lower than that. It's just not
>> guaranteed in the spec and it may differ from one Si571 sample to another.
>> I assume Silicon Labs had a pretty good reason for specifying the lower limit as
>> 10 MHz.
>>
>> By the way, I assume that the reason why you want to use a Si571 rather than
>> a Si570 is because you already have one sample part. That's fine. For this
>> application there really isn't any advantage in being able to "pull" the frequency
>> by applying a voltage to the VCXO pin so the Si571 (VCXO) really isn't an
>> advantage over the Si570 (XO).. (The voltage-control pin is not connected in

>> the Si570.) The VCXO voltage will affect the calibration and you will have to
>> add some additional circuitry to manually vary that voltage to calibrate the
>> frequency. In the Si570 the calibration can all be done in software.
>>
>> Best Regards,
>> -Craig, AA0ZZ
>>
>>
>
> Thanks Craig,
> The reason for the use of the Si571 is I want to use it as an FM
> modulator.
> Generating FM at 9 MHz is not easy, the range becomes limited by the
> varicap diode characteristics which limits the modulation freq.
> The Si571 doesn't gave those problems, and should be very linear .
>>
>
>
> --
> Best wishes / 73
> Richard Bown
>
> E-mail: richard@...
>
> nil carborundum a illegitemis
> ##
> Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
> Ham Call:G8JVM
> Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
> QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
> ##
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
>
>
>

155. Re: [PPLL-VFO] Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 16:42:52 UTC
From: Francis DUPONT
Topic: 144 Message: 155

Hi Richard,

Sorry if my explanations were not clear enough. English is not my native language...

< ...dont want to have to connect to the computer via USB to
< set the frequency.

Of course. You need only the PC and the USB link for the first calibration and to set "your" frequency.
After that, these 2 parameters are stored in the ATtiny85 EEPROM.

< Do you know if the startup frequency can be put in the ATMEL device.

At each power up, the firmware is able to use them, and you get "your frequency".

If a few months later you want to use another frequency, just plug the USB cable to modify the frequency.

I have not used the words "start-up frequency" to avoid any confusion with the factory start-up frequency which cannot be modified by the user.

If you need more details, I will try to answer.

Best Regards,

Francis

156. Si570_VFO_Code

Yahoo group: PPLL-VFO
Date: 2011-09-18 17:56:37 UTC
From: k5dnl
Topic: 156 Message: 156

Hello all,

I'm trying to build a vfo using the Si570 chip for home brew
4 band superhet receiver , I have a few pic's , 16F676 , 16F628,
16F886 and a CanaKit programmer.
Can someone direct me to a link that I can download the source
Code for anyone of these pic chips for a simple stand alone VFO.

I'm trying to learn Pic programming but it's still over my head.
Thanks 73 Ken K5DNL

157. Re: [PPLL-VFO] Si570_VFO_Code

Yahoo group: PPLL-VFO
Date: 2011-09-18 20:04:03 UTC
From: Justin Pinnix
Topic: 156 Message: 157

Hi Ken,

Craig's code should be a good starting point - he has asm source available at http://cbjohn.com/aa0zz/index.html. You will want to hook up your 570 and controls the same way he did his, otherwise you'll have to modify the code.

73 de aj4mj

On Sunday, September 18, 2011, k5dnl <kwroberson@yahoo.com> wrote:
>
>
> Hello all,
>
> I'm trying to build a vfo using the Si570 chip for home brew
> 4 band superhet receiver , I have a few pic's , 16F676 , 16F628,
> 16F886 and a CanaKit programmer.
> Can someone direct me to a link that I can download the source
> Code for anyone of these pic chips for a simple stand alone VFO.
>
> I'm trying to learn Pic programming but it's still over my head.
> Thanks 73 Ken K5DNL
>
>

158. Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-18 21:24:35 UTC
From: mikewogden
Topic: 144 Message: 158

Richard

try this

http://g4oep.atspace.com/channels/channels.htm

It should be what your looking for

Regards

Mike G4KXQW

159. Re: [PPLL-VFO] Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-19 09:06:19 UTC
From: Richard
Topic: 144 Message: 159

On Sun, 2011-09-18 at 21:24 +0000, mikewogden wrote:
>
>
>
> Richard
>
> try this
>
> http://g4oep.atspace.com/channels/channels.htm
>
> It should be what your looking for
>
> Regards
>
> Mike G4KXQW
>
Hi Mike
thats exactly what I was looking for.
Thanks

--
Best wishes / 73
Richard Bown

E-mail: richard@...

nil carborundum a illegitemis
##
Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
Ham Call:G8JVM
Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
##

160. Control board band decode

Yahoo group: PPLL-VFO
Date: 2011-09-19 15:30:29 UTC
From: k5dnl
Topic: 160 Message: 160

Hello All,

Started to order the Control and daughter board ,
But did not find an output from the Pic for band decode ?
I need BCD output to decode for pass band filters.

Ken K5DNL

161. Re: [PPLL-VFO] Control board band decode

Yahoo group: PPLL-VFO
Date: 2011-09-19 23:15:43 UTC
From: Craig Johnson, AA0ZZ
Topic: 160 Message: 161

Ken,

Yes, that is true. Those 24 bands used in the application are internal only and do not correspond to
ham bands so it may be confusing anyway. The main problem is that it would require 5 bits to output
the band number (0 to 23) in binary and it would require more bits to put out in BCD. There are no
unused pins on this tiny PIC.

Best Regards,
-Craig

----- Original Message -----
From: "k5dnl" <kwroberson@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, September 19, 2011 10:30 AM
Subject: [PPLL-VFO] Control board band decode

> Hello All,
>
> Started to order the Control and daughter board ,
> But did not find an output from the Pic for band decode ?
> I need BCD output to decode for pass band filters.
>
> Ken K5DNL
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
>
>
>

162. Re: Single frequency loading on Si571

Yahoo group: PPLL-VFO
Date: 2011-09-20 15:59:40 UTC
From: mikewogden
Topic: 144 Message: 162

That's Ok

Lots of interesting PIC based projects and a quick personal response to any questions.

Regards

Mike

G4KXQ

--- In PPLL-VFO@yahoogroups.com, Richard <richard@...> wrote:
>
> On Sun, 2011-09-18 at 21:24 +0000, mikewogden wrote:
> >
> >
> >
> > Richard
> >
> > try this
> >
> > http://g4oep.atspace.com/channels/channels.htm
> >
> > It should be what your looking for
> >
> > Regards
> >
> > Mike G4KXQW
> >
> Hi Mike
> thats exactly what I was looking for.
> Thanks
>
> --
> Best wishes / 73
> Richard Bown
>
> E-mail: richard@...
>
> nil carborundum a illegitemis
> ##
> Sent by Evolution 2.32.1 on Fedora FC15 x86_64 Dual core AMD Athlon 4400
> Ham Call:G8JVM
> Maidenhead QRA: IO82SP38:LAT. 52 39.720':N LONG. 2 28.171 W (degs,mins)
> QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3 cms:5W
> ##
>

164. W6JL receiver circuit boards

Yahoo group: PPLL-VFO
Date: 2011-11-16 21:20:09 UTC
From: jimhwallace
Topic: 164 Message: 164

I'll be getting a Si570 VFO kit, and I'd like to build a good receiver to go with it. Are circuit board Express schematics or layouts or actual circuit boards for W6JL's receiver available anywhere? If not, would I be out of line posting layouts here if I develop my own? Or, is there a better forum for this issue? I looked quite a bit and didn't find any place more suitable.

The VFO or the receiver will be my first SMT project, so I'd rather not do it dead-bug style. I've built a lot before this. I did see the MicroR2 front end files and I've been through all the W6JL and AA0ZZ web stuff (at least I think I've seen it all).

Jim, KB5MT

165. Re: W6JL receiver circuit boards

Yahoo group: PPLL-VFO
Date: 2011-11-19 01:07:39 UTC
From: AA0ZZ
Topic: 164 Message: 165

Hi Jim,

Board designs that are posted here are intended for others to look at and try. Making a board using designs posted here are certainly permissiable and we would certainly like to hear about yout experiences. Yes, you can even post a layout for others to try. It's just if you intend to make these boards to sell to others that could be a problem. You should ask for the designer's permission before you do that.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "jimhwallace" <jimandcathywallace@...> wrote:
>
> I'll be getting a Si570 VFO kit, and I'd like to build a good receiver to go with it. Are circuit board Express schematics or layouts or actual circuit boards for W6JL's receiver available anywhere? If not, would I be out of line posting layouts here if I develop my own? Or, is there a better forum for this issue? I looked quite a bit and didn't find any place more suitable.
>
> The VFO or the receiver will be my first SMT project, so I'd rather not do it dead-bug style. I've built a lot before this. I did see the MicroR2 front end files and I've been through all the W6JL and AA0ZZ web stuff (at least I think I've seen it all).
>
> Jim, KB5MT
>

166. Re: W6JL receiver circuit boards

Yahoo group: PPLL-VFO
Date: 2011-11-19 01:10:13 UTC
From: AA0ZZ
Topic: 164 Message: 166

Make that "permissible". Good grief.

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Hi Jim,
>
> Board designs that are posted here are intended for others to look at and try. Making a board using designs posted here are certainly permissiable and we would certainly like to hear about yout experiences. Yes, you can even post a layout for others to try. It's just if you intend to make these boards to sell to others that could be a problem. You should ask for the designer's permission before you do that.
>
> Best Regards,
> -Craig, AA0ZZ
>
> --- In PPLL-VFO@yahoogroups.com, "jimhwallace" <jimandcathywallace@> wrote:
> >
> > I'll be getting a Si570 VFO kit, and I'd like to build a good receiver to go with it. Are circuit board Express schematics or layouts or actual circuit boards for W6JL's receiver available anywhere? If not, would I be out of line posting layouts here if I develop my own? Or, is there a better forum for this issue? I looked quite a bit and didn't find any place more suitable.
> >
> > The VFO or the receiver will be my first SMT project, so I'd rather not do it dead-bug style. I've built a lot before this. I did see the MicroR2 front end files and I've been through all the W6JL and AA0ZZ web stuff (at least I think I've seen it all).
> >
> > Jim, KB5MT
> >
>

167. IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-20 12:06:25 UTC
From: nikolaresler
Topic: 167 Message: 167

TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.

I'm using symmetric if filter with center xtal of 5645 for usb filter 5645+2.4 kHz lsb filter 5645 -2.4khc.(DRAKE filters maybe) if shift in dis case pointed to center frequency on 5645 exact.So I haw USB and LSB swishing filters .Understand weary well gm4toe s file , A3 44 E0 10.700.000 and 56 22 C8 5.645.000 . Simple to ad to program without switch on off like in old dds need for button on off is exhausted.

Where to ad gm4toe s file in which line exact in Craig's asembler ???

And my work is coming to end! Tnx. AA0ZZ and GM4TOE de ex 4N7RN (almost everything is ex in my country HI!) 73 ! Nikola

168. Re: [PPLL-VFO] IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-20 17:33:46 UTC
From: Craig Johnson, AA0ZZ
Topic: 167 Message: 168

Hello, Nikola.

I am glad to see that you posted your request here for all of us to think about.

First we need to understand exactly what you are looking for. If I don't understand it; maybe you or someone else can help us. I
could not find the file from GM4TOE that has more information about this. Perhaps you could give a specific location for that file.

If I understand correctly, you are looking for code that adds (5645000 + 2400 Hz if USB) or (5645000 - 2400 if LSB) to the base
Si570 and display frequency. Is this correct? Then you also want the option to use another case in which the code adds (5645+2400
Hz if USB) or (5645-2400 Hz if LSB). Correct?

The code to do this would NOT use the "tone" code since the tone is the shift amount that is added when in Receive mode and is not
added when in Transmit mode. You want it for an IF frequency which is always added to the base frequency. Then 2400 Hz would
always be added to the base frequency if the mode is USB and always subtracted if it is LSB. Is this correct?

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "nikolaresler" <nikolaresler@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, November 20, 2011 6:06 AM
Subject: [PPLL-VFO] IF shift

> TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.
>
>
> I'm using symmetric if filter with center xtal of 5645 for usb filter 5645+2.4 kHz lsb filter 5645 -2.4khc.(DRAKE filters maybe)
> if shift in dis case pointed to center frequency on 5645 exact.So I haw USB and LSB swishing filters .Understand weary well
> gm4toe s file , A3 44 E0 10.700.000 and 56 22 C8 5.645.000 . Simple to ad to program without switch on off like in old dds
> need for button on off is exhausted.
>
> Where to ad gm4toe s file in which line exact in Craig's asembler ???
>
> And my work is coming to end! Tnx. AA0ZZ and GM4TOE de ex 4N7RN (almost everything is ex in my country HI!) 73 ! Nikola

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> Yahoo! Groups Links
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169. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-20 20:29:04 UTC
From: nikolaresler
Topic: 167 Message: 169

http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/

if this file can put in Ur assembler or not ?

I'm using 2 if filters
1. 5.645.002,4 usb filter
2. 5.644.997,6 lsb filter
3. BFO xtal freq 5.645.000

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hello, Nikola.
>
> I am glad to see that you posted your request here for all of us to think about.
>
> First we need to understand exactly what you are looking for. If I don't understand it; maybe you or someone else can help us. I
> could not find the file from GM4TOE that has more information about this. Perhaps you could give a specific location for that file.
>
> If I understand correctly, you are looking for code that adds (5645000 + 2400 Hz if USB) or (5645000 - 2400 if LSB) to the base
> Si570 and display frequency. Is this correct? Then you also want the option to use another case in which the code adds (5645+2400
> Hz if USB) or (5645-2400 Hz if LSB). Correct?
>
> The code to do this would NOT use the "tone" code since the tone is the shift amount that is added when in Receive mode and is not
> added when in Transmit mode. You want it for an IF frequency which is always added to the base frequency. Then 2400 Hz would
> always be added to the base frequency if the mode is USB and always subtracted if it is LSB. Is this correct?
>
> Best Regards,
> -Craig, AA0ZZ
>
>
> ----- Original Message -----
> From: "nikolaresler" <nikolaresler@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Sunday, November 20, 2011 6:06 AM
> Subject: [PPLL-VFO] IF shift
>
>
> > TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.

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> > I'm using symmetric if filter with center xtal of 5645 for usb filter 5645+2.4 kHz lsb filter 5645 -2.4khc.(DRAKE filters maybe)
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> >
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> > Yahoo! Groups Links
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170. Re: [PPLL-VFO] Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-21 06:52:46 UTC
From: John Kolb
Topic: 167 Message: 170

The numbers below look wrong, being 2.4 Hz above or below the BFO
freq, not 2.4 kHz,
representing the filter bandwidth.

The next question is should the display indicate the frequency of the
suppressed
carrier, in which case, the offset for the display would be 5.645.000
Hz for either LSB
or USB. To display the center freq, the offset would be 5.645.000 Hz
+ or - 1200 Hz
depending on sideband.

I'd try tuning in known freq SSB stations,both LSB and USB, without
an offset, and see
what the actual display error is.

John
KK6IL

At 12:29 PM 11/20/2011, you wrote:

>http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
>
>if this file can put in Ur assembler or not ?
>
>I'm using 2 if filters
>1. 5.645.002,4 usb filter
>2. 5.644.997,6 lsb filter
>3. BFO xtal freq 5.645.000
>
>

171. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-21 07:24:39 UTC
From: nikolaresler
Topic: 167 Message: 171

Yes the center carrier freq! The offset for the display is + 5.645.000,higher Nothing else.

--- In PPLL-VFO@yahoogroups.com, John Kolb <jlkolb@...> wrote:
>
>
> The numbers below look wrong, being 2.4 Hz above or below the BFO
> freq, not 2.4 kHz,
> representing the filter bandwidth.
>
> The next question is should the display indicate the frequency of the
> suppressed
> carrier, in which case, the offset for the display would be 5.645.000
> Hz for either LSB
> or USB. To display the center freq, the offset would be 5.645.000 Hz
> + or - 1200 Hz
> depending on sideband.
>
> I'd try tuning in known freq SSB stations,both LSB and USB, without
> an offset, and see
> what the actual display error is.
>
> John
> KK6IL
>
>
> At 12:29 PM 11/20/2011, you wrote:
>
> >http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
> >
> >if this file can put in Ur assembler or not ?
> >
> >I'm using 2 if filters
> >1. 5.645.002,4 usb filter
> >2. 5.644.997,6 lsb filter
> >3. BFO xtal freq 5.645.000
> >
> >
>

172. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-21 07:59:44 UTC
From: nikolaresler
Topic: 167 Message: 172

--- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@...> wrote:
> http://img3.imageshack.us/img3/7120/43610817.gif
> Yes the center carrier freq! The offset for the display is + 5.645.000,higher Nothing else.
>
> --- In PPLL-VFO@yahoogroups.com, John Kolb <jlkolb@> wrote:
> >
> >
> > The numbers below look wrong, being 2.4 Hz above or below the BFO
> > freq, not 2.4 kHz,
> > representing the filter bandwidth.
> >
> > The next question is should the display indicate the frequency of the
> > suppressed
> > carrier, in which case, the offset for the display would be 5.645.000
> > Hz for either LSB
> > or USB. To display the center freq, the offset would be 5.645.000 Hz
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> > I'd try tuning in known freq SSB stations,both LSB and USB, without
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> > John
> > KK6IL
> >
> >
> > At 12:29 PM 11/20/2011, you wrote:
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> > >1. 5.645.002,4 usb filter
> > >2. 5.644.997,6 lsb filter
> > >3. BFO xtal freq 5.645.000
> > >
> > >
> >
> >
>

173. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-22 19:15:51 UTC
From: AA0ZZ
Topic: 167 Message: 173

Nikola,
The bin2BCD code affects only the display frequency, not the Si570 frequency. I think you want to change the Si570 frequency (add the IF frequency amount) without changing the display frequency.
Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@...> wrote:
>
>
>
> http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
>
> if this file can put in Ur assembler or not ?
>
> I'm using 2 if filters
> 1. 5.645.002,4 usb filter
> 2. 5.644.997,6 lsb filter
> 3. BFO xtal freq 5.645.000
>
>
>
> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >
> > Hello, Nikola.
> >
> > I am glad to see that you posted your request here for all of us to think about.
> >
> > First we need to understand exactly what you are looking for. If I don't understand it; maybe you or someone else can help us. I
> > could not find the file from GM4TOE that has more information about this. Perhaps you could give a specific location for that file.
> >
> > If I understand correctly, you are looking for code that adds (5645000 + 2400 Hz if USB) or (5645000 - 2400 if LSB) to the base
> > Si570 and display frequency. Is this correct? Then you also want the option to use another case in which the code adds (5645+2400
> > Hz if USB) or (5645-2400 Hz if LSB). Correct?
> >
> > The code to do this would NOT use the "tone" code since the tone is the shift amount that is added when in Receive mode and is not
> > added when in Transmit mode. You want it for an IF frequency which is always added to the base frequency. Then 2400 Hz would
> > always be added to the base frequency if the mode is USB and always subtracted if it is LSB. Is this correct?

> >
> > Best Regards,
> > -Craig, AA0ZZ
> >
> >
> > ----- Original Message -----
> > From: "nikolaresler" <nikolaresler@>
> > To: <PPLL-VFO@yahoogroups.com>
> > Sent: Sunday, November 20, 2011 6:06 AM
> > Subject: [PPLL-VFO] IF shift
> >
> >
> > > TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.
> > >
> > >
> > > I'm using symmetric if filter with center xtal of 5645 for usb filter 5645+2.4 kHz lsb filter 5645 -2.4khc.(DRAKE filters maybe)
> > > if shift in dis case pointed to center frequency on 5645 exact.So I haw USB and LSB swishing filters .Understand weary well
> > > gm4toe s file , A3 44 E0 10.700.000 and 56 22 C8 5.645.000 . Simple to ad to program without switch on off like in old dds
> > > need for button on off is exhausted.
> > >
> > > Where to ad gm4toe s file in which line exact in Craig's asembler ???
> > >
> > > And my work is coming to end! Tnx. AA0ZZ and GM4TOE de ex 4N7RN (almost everything is ex in my country HI!) 73 ! Nikola
> > >
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> > > Yahoo! Groups Links
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174. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-22 19:39:08 UTC
From: nikolaresler
Topic: 167 Message: 174

Yes change the Si570 frequency (add the IF frequency amount)
without changing the display frequency.
Yes example, display is on 10.000.000 Hc and Si570 frequency is higher 5.654.000 Hc,on 15.645.000 .

>
>
> Nikola,
> The bin2BCD code affects only the display frequency, not the Si570 frequency. I think you want to change the Si570 frequency (add the IF frequency amount) without changing the display frequency.
> Best Regards,
> -Craig, AA0ZZ
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>
> --- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@> wrote:
> >
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> >
> > http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
> >
> > if this file can put in Ur assembler or not ?
> >
> > I'm using 2 if filters
> > 1. 5.645.002,4 usb filter
> > 2. 5.644.997,6 lsb filter
> > 3. BFO xtal freq 5.645.000
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> >
> > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> > >
> > > Hello, Nikola.
> > >
> > > I am glad to see that you posted your request here for all of us to think about.
> > >
> > > First we need to understand exactly what you are looking for. If I don't understand it; maybe you or someone else can help us. I
> > > could not find the file from GM4TOE that has more information about this. Perhaps you could give a specific location for that file.
> > >
> > > If I understand correctly, you are looking for code that adds (5645000 + 2400 Hz if USB) or (5645000 - 2400 if LSB) to the base
> > > Si570 and display frequency. Is this correct? Then you also want the option to use another case in which the code adds (5645+2400

> > > Hz if USB) or (5645-2400 Hz if LSB). Correct?
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> > > The code to do this would NOT use the "tone" code since the tone is the shift amount that is added when in Receive mode and is not
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> > > -Craig, AA0ZZ
> > >
> > >
> > > ----- Original Message -----
> > > From: "nikolaresler" <nikolaresler@>
> > > To: <PPLL-VFO@yahoogroups.com>
> > > Sent: Sunday, November 20, 2011 6:06 AM
> > > Subject: [PPLL-VFO] IF shift
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> > > > TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.
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> > > > gm4toe s file , A3 44 E0 10.700.000 and 56 22 C8 5.645.000 . Simple to ad to program without switch on off like in old dds
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> > > > Where to ad gm4toe s file in which line exact in Craig's asembler ???
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> > > > And my work is coming to end! Tnx. AA0ZZ and GM4TOE de ex 4N7RN (almost everything is ex in my country HI!) 73 ! Nikola
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> > > > Yahoo! Groups Links
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175. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-22 21:03:55 UTC
From: AA0ZZ
Topic: 167 Message: 175

Then bin2BCD is not the place to do it.
-Craig

--- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@...> wrote:
>
>
> Yes change the Si570 frequency (add the IF frequency amount)
> without changing the display frequency.
> Yes example, display is on 10.000.000 Hc and Si570 frequency is higher 5.654.000 Hc,on 15.645.000 .
>
> >
> >
> > Nikola,
> > The bin2BCD code affects only the display frequency, not the Si570 frequency. I think you want to change the Si570 frequency (add the IF frequency amount) without changing the display frequency.
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> > --- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@> wrote:
> > >
> > >
> > >
> > > http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
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> > > if this file can put in Ur assembler or not ?
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> > > I'm using 2 if filters
> > > 1. 5.645.002,4 usb filter
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> > > 3. BFO xtal freq 5.645.000
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> > >
> > >
> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> > > >
> > > > Hello, Nikola.
> > > >
> > > > I am glad to see that you posted your request here for all of us to think about.
> > > >
> > > > First we need to understand exactly what you are looking for. If I don't understand it; maybe you or someone else can help us. I
> > > > could not find the file from GM4TOE that has more information about this. Perhaps

you could give a specific location for that file.
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> > > > If I understand correctly, you are looking for code that adds (5645000 + 2400 Hz if USB) or (5645000 - 2400 if LSB) to the base
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> > > > The code to do this would NOT use the "tone" code since the tone is the shift amount that is added when in Receive mode and is not
> > > > added when in Transmit mode. You want it for an IF frequency which is always added to the base frequency. Then 2400 Hz would
> > > > always be added to the base frequency if the mode is USB and always subtracted if it is LSB. Is this correct?
> > > >
> > > > Best Regards,
> > > > -Craig, AA0ZZ
> > > >
> > > >
> > > > ----- Original Message -----
> > > > From: "nikolaresler" <nikolaresler@>
> > > > To: <PPLL-VFO@yahoogroups.com>
> > > > Sent: Sunday, November 20, 2011 6:06 AM
> > > > Subject: [PPLL-VFO] IF shift
> > > >
> > > >
> > > > > TNX Craig your Si 570 working fine ! Tnx for membership on YAHOO ! I'm surprised on many suggestion.My problem was IF shift.
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> > > > > I'm using symmetric if filter with center xtal of 5645 for usb filter 5645+2.4 kHz lsb filter 5645 -2.4khc.(DRAKE filters maybe)
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> > > > > And my work is coming to end! Tnx. AA0ZZ and GM4TOE de ex 4N7RN (almost everything is ex in my country HI!) 73 ! Nikola
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> > > > > Yahoo! Groups Links
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176. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-22 18:02:00 UTC
From: gm4toe
Topic: 167 Message: 176

My routine, in the files section, adds in a shift to the displayed frequency to allow for the IF. Insert the code immediately after the header for the sub routine "bin2BCD". It is set for an IF of 10.7MHz (if I remember correctly) so it is necessary to modify the hex values in the following lines:

movlw 0xE0 ;add LSB of IF shift

movlw 0x44 ;put next byte of IF in W reg

movlw 0xA3 ;third byte of IF shift

If you need any help please let me know

Regards

Barry GM4TOE

--- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@...> wrote:
>
>
>
>
>
> --- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@> wrote:
> > http://img3.imageshack.us/img3/7120/43610817.gif
> > Yes the center carrier freq! The offset for the display is + 5.645.000,higher Nothing else.
> >
> > --- In PPLL-VFO@yahoogroups.com, John Kolb <jlkolb@> wrote:
> > >
> > >
> > > The numbers below look wrong, being 2.4 Hz above or below the BFO
> > > freq, not 2.4 kHz,
> > > representing the filter bandwidth.
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> > > The next question is should the display indicate the frequency of the
> > > suppressed
> > > carrier, in which case, the offset for the display would be 5.645.000
> > > Hz for either LSB
> > > or USB. To display the center freq, the offset would be 5.645.000 Hz
> > > + or - 1200 Hz
> > > depending on sideband.
> > >
> > > I'd try tuning in known freq SSB stations,both LSB and USB, without
> > > an offset, and see
> > > what the actual display error is.
> > >

> > > John
> > > KK6IL
> > >
> > >
> > > At 12:29 PM 11/20/2011, you wrote:
> > >
> > > >http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
> > > >
> > > >if this file can put in Ur assembler or not ?
> > > >
> > > >I'm using 2 if filters
> > > >1. 5.645.002,4 usb filter
> > > >2. 5.644.997,6 lsb filter
> > > >3. BFO xtal freq 5.645.000
> > > >
> > > >
> > >
> >
>

177. Re: IF shift

Yahoo group: PPLL-VFO
Date: 2011-11-23 19:32:45 UTC
From: AA0ZZ
Topic: 167 Message: 177

OK. If you simply want the Display frequency to be different than the Si570 frequency by a constant amount, then this may be sufficient. I haven't tried it myself.
Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@...m, "gm4toe" <barryhorning@...> wrote:
>
> My routine, in the files section, adds in a shift to the displayed frequency to allow for the IF. Insert the code immediately after the header for the sub routine "bin2BCD". It is set for an IF of 10.7MHz (if I remember correctly) so it is necessary to modify the hex values in the following lines:
>
> movlw 0xE0 ;add LSB of IF shift
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> movlw 0x44 ;put next byte of IF in W reg
>
> movlw 0xA3 ;third byte of IF shift
>
> If you need any help please let me know
>
> Regards
>
> Barry GM4TOE
>
>
>
>
> --- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@> wrote:
> >
> >
> >
> >
> >
> > --- In PPLL-VFO@yahoogroups.com, "nikolaresler" <nikolaresler@> wrote:
> > > http://img3.imageshack.us/img3/7120/43610817.gif
> > > Yes the center carrier freq! The offset for the display is + 5.645.000,higher Nothing else.
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> > > --- In PPLL-VFO@yahoogroups.com, John Kolb <jlkolb@> wrote:
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> > > > The numbers below look wrong, being 2.4 Hz above or below the BFO
> > > > freq, not 2.4 kHz,
> > > > representing the filter bandwidth.
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> > > > The next question is should the display indicate the frequency of the
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> > > > At 12:29 PM 11/20/2011, you wrote:
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> > > > >http://groups.yahoo.com/group/PPLL-VFO/files/IF%20Shift/
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> > > > >I'm using 2 if filters
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> > > > >3. BFO xtal freq 5.645.000
> > > > >
> > > > >
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178. Restricting the range of the VFO

Yahoo group: PPLL-VFO
Date: 2011-11-28 20:31:04 UTC
From: gm4toe
Topic: 178 Message: 178

I would like to restrict the range covered by the VFO rather than the 10 to 150MHz (or thereabouts) that it does at the moment. I just can't seem to get my head around the code and how to restrict it (say make it only tune from 30 to 70MHz). I am sure it is blatantly obvious, but my quantity of brain cells is being eroded!!

Any pointers to where I should be looking please

Many thanks

Barry GM4TOE

179. Re: Restricting the range of the VFO

Yahoo group: PPLL-VFO
Date: 2011-12-05 03:47:41 UTC
From: AA0ZZ
Topic: 178 Message: 179

Barry,
Sorry about the slow response.
To change the lower limit just change the constants LLIMIT_3 .. LLIMIT_0. To change the upper limit just change the constants ULIMIT_3..ULIMIT_0. That should do it.
Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "gm4toe" <barryhorning@...> wrote:
>
> I would like to restrict the range covered by the VFO rather than the 10 to 150MHz (or thereabouts) that it does at the moment. I just can't seem to get my head around the code and how to restrict it (say make it only tune from 30 to 70MHz). I am sure it is blatantly obvious, but my quantity of brain cells is being eroded!!
>
> Any pointers to where I should be looking please
>
> Many thanks
>
> Barry GM4TOE
>

180. Re: Restricting the range of the VFO

Yahoo group: PPLL-VFO
Date: 2011-12-05 11:15:12 UTC
From: gm4toe
Topic: 178 Message: 180

Hi Craig

Enter here a quote from Homer Simpson:"..."

I had a horrid feeling it was blatantly obvious and I should have spotted it. Maybe I should take up flower arranging!

Many thanks for your help

Barry GM4TOE

--- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@...> wrote:
>
> Barry,
> Sorry about the slow response.
> To change the lower limit just change the constants LLIMIT_3 .. LLIMIT_0. To change the upper limit just change the constants ULIMIT_3..ULIMIT_0. That should do it.
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> -Craig, AA0ZZ
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> >
> > Any pointers to where I should be looking please
> >
> > Many thanks
> >
> > Barry GM4TOE
> >
>

181. Re: [PPLL-VFO] Re: Restricting the range of the VFO

Yahoo group: PPLL-VFO
Date: 2011-12-05 12:46:08 UTC
From: Craig Johnson, AA0ZZ
Topic: 178 Message: 181

Barry,
No need to change hobbies! Glad I was able to help.
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "gm4toe" <barryhorning@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, December 05, 2011 5:15 AM
Subject: [PPLL-VFO] Re: Restricting the range of the VFO

> Hi Craig
>
> Enter here a quote from Homer Simpson:"..."
>
> I had a horrid feeling it was blatantly obvious and I should have spotted it. Maybe I should take up flower arranging!
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>>
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>> > is blatantly obvious, but my quantity of brain cells is being eroded!!
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>> > Any pointers to where I should be looking please
>> >
>> > Many thanks

>> >
>> > Barry GM4TOE
>> >
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>
> Yahoo! Groups Links
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182. CW Transmitter Circuit

Yahoo group: PPLL-VFO
Date: 2012-01-07 03:43:09 UTC
From: justinpinnix
Topic: 182 Message: 182

Hi Folks,

I'm curious about the example 40 meter CW TX circuit listed in the article. Is it based on a circuit from somewhere else that I can read up on? How much power does it put out? Other than the output filters, are other parts of the circuit band-specific?

73 de AJ4MJ

184. Re: CW Transmitter Circuit

Yahoo group: PPLL-VFO
Date: 2012-01-07 20:55:58 UTC
From: AA0ZZ
Topic: 182 Message: 184

Hi Justin,

Interesting question. It's time for an update / discussion about that circuit anyway.

No, you won't find this circuit elsewhere; it is a creation of mine, but it is based on ideas from many sources.

I would suggest that you pick up the latest version (v2b) of the transmitter - now in the FILES section and on my web page. While the original circuit probably works, it has some flaws in the divide-by-4 portion that should be corrected.

1) The 74AC74 should not be run at 12v; 5v is much preferable.

2) The the output of the Si570 is about 1.5v p-p. While this is enough to drive the 74AC74 flip flops in many cases, it isn't quite enough according to the spec sheet. If the device is powered with 5v, the spec says a "high" should be above 3.4v and a "low" should be below 1.5v. Swinging the Si570 from zero to 1.5v will probably be OK to trigger the flip flops in most 74AC74 chips it isn't guaranteed and that means it really isn't a good, robust, works-in-all-cases design.

I have corrected these flaws in the latest version of the circuit. Now the Si570 feeds into a pair of "Exclusive OR" gates and uses a trick that Don, W6JL, taught me. The assumption is that both of the XOR gates on any given part have the same "center" switching point. The input is terminated at 51 ohms and then fed to the bottom XOR gate (U9b) which biases the input signal in the very center of the switching range of this particular pair of gates (near 2.5v). The
centered signal is fed to the other XOR gate (U9a) and now a very small voltage swing will activate it. Now our 1.5v p-p signal will work it very nicely. R51, the 5.1k resistor, keeps the gate input offset a bit away from the center so that the gate will not oscillate. Different values can be used for R51, depending on how much sensivity is needed.

This works very nicely. I'm now playing with various types of low pass filters for this circuit. The given LPF should work fine for 40 meters (7.0 MHz) and other LPFs can be switched in, using a mechanism of your choosing, for other bands. It appears that these particular XOR gates and flip-flops will not be sufficient to go higher than 21 MHz or so. Transmitter output with the three 2N2222's is about 1.5 watts (34v p-p). For the final 2N2222s you should use metal can 2N2222A's with heat sink "hats" for best performance. Also resistor R16 is passing a lot of current so you may want to use a 1/2 or 1 watt resistor there. This is not designed for holding the key down for very long period of time. If you do, please report what "smokes" first! Also, be very sure you have a dummy load or antenna connected as it needs a 50 ohm load.

By the way, the same XOR switching scheme should be used for the receivers that are driven by the Si570 and the divide-by-4 mechanism. I haven't updated all of the diagrams yet.

Let me know if you have questions.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "justinpinnix" <justin.pinnix@...> wrote:
>
> Hi Folks,
>
> I'm curious about the example 40 meter CW TX circuit listed in the article. Is it based on a circuit from somewhere else that I can read up on? How much power does it put out? Other than the output filters, are other parts of the circuit band-specific?
>
> 73 de AJ4MJ
>

185. Re: [PPLL-VFO] CW Transmitter Circuit

Yahoo group: PPLL-VFO
Date: 2012-01-08 03:22:46 UTC
From: Justin Pinnix
Topic: 182 Message: 185

Thanks Craig for the update and the info.

1.5 watts should be perfect. I'm planning on feeding my W6JL amp with it (the homebrew challenge winner).

One followup question - Is the mixing of AC and HC logic families intentional, or just the result of the circuit evolving over time?

73 de aj4mj

On Saturday, January 7, 2012, AA0ZZ <aa0zz@...> wrote:
>
>
> Hi Justin,
>
> Interesting question. It's time for an update / discussion about that circuit anyway.
>
> No, you won't find this circuit elsewhere; it is a creation of mine, but it is based on ideas from many sources.
>
> I would suggest that you pick up the latest version (v2b) of the transmitter - now in the FILES section or from my web page.
> While the original circuit probably works, it has some flaws in the divide-by-4 portion that should be corrected.
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> 1) The 74AC74 should not be run at 12v; 5v is much preferable.
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> 2) The the output of the Si570 is about 1.5v p-p. While this is enough to drive the 74AC74 flip flops in many cases, it isn't quite enough according to the spec sheet. If the device is powered with 5v, the spec says a "high" should be above 3.4v and a "low" should be below 1.5v. Swinging the Si570 from zero to 1.5v will probably be OK to trigger the flip flops in most 74AC74 chips it isn't guaranteed and that means it really isn't a good, robust, works-in-all-cases design.
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> By the way, the same XOR switching scheme should be used for the receivers that are driven by the Si570 and the divide-by-4 mechanism. I haven't updated all of the diagrams yet.
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> --- In PPLL-VFO@yahoogroups.com, "justinpinnix" <justin.pinnix@...> wrote:
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>> Hi Folks,
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>>
>> 73 de AJ4MJ
>>
>
>

186. Re: [PPLL-VFO] CW Transmitter Circuit

Yahoo group: PPLL-VFO
Date: 2012-01-08 03:37:39 UTC
From: Craig Johnson, AA0ZZ
Topic: 182 Message: 186

Justin,

No particular reason for mixing the logic families. It's an example design, and I am sure other components can be used.
Maybe some will work better. Maybe some parts will allow 30 MHz operation.

Hey, folks. Try other parts and designs and let us know what you find! That is what this group is for.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: Justin Pinnix
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, January 07, 2012 9:22 PM
Subject: Re: [PPLL-VFO] CW Transmitter Circuit

Thanks Craig for the update and the info.

1.5 watts should be perfect. I'm planning on feeding my W6JL amp with it (the homebrew challenge winner).

One followup question - Is the mixing of AC and HC logic families intentional, or just the result of the circuit evolving over time?

73 de aj4mj

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> No, you won't find this circuit elsewhere; it is a creation of mine, but it is based on ideas from many sources.
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>> 73 de AJ4MJ
>>
>
>

187. Re: [PPLL-VFO] Re: CW Transmitter Circuit

Yahoo group: PPLL-VFO
Date: 2012-01-09 23:13:02 UTC
From: Jim or Cathy Wallace
Topic: 182 Message: 187

This is a little premature but perhaps a good enough time to give a heads-up. I've been fascinated with Craig's (et all) quadrature receiver design and intend to build it soon. Before the holidays I spent several days intensely capturing the schematic and making a parts layout. It seems about ready to publish, and I'm perfectly glad to do that, especially since there now seems to be interest in making the transmitter version of the front end. The two are, perhaps, identical, so a board layout would be useful to transmitter builders as well--at least as a starting point.

There are some shortcomings. Exchange, the software that I know best for this, does not have surface mount parts and there are other limitations. Somehow I stumbled onto DipTrace (http://www.diptrace.com/) which had the parts and seemed good for the job. That's what I used. There's a free version, and it's powerful though harder to learn than Exchange, and different. Also, its files are in a proprietary format, at least as far as I know. There's no export to PDF, TIFF, jpg, or some portable format. It does do Gerber files.

I did the receiver files for two boards, one for RF through I-Q output, and the other for minimal audio processing, Both are rather small but not crowded. I'm not sure yet about some details, like bypass capacitors, and component selection is pretty crude, based mostly on the pattern library instead of parts catalog and preferred spacing for common sizes. It does use the OR's that Craig speaks of and shows. Reference designators are different than those used elsewhere.

I'll check it some more and post the files in a few days, but be aware that I have not built any of this stuff, yet. It'll surely change when I do, and that will probably be months from now. Thus, I'll be anxious to hear comments and improvements from those that get ahead of me. I love to build, but I don't seem to get much of it done these days. I won't be doing boards for sale. I'm not even sure how I'll do my own.

Best Wishes,
Jim Wallace
KB5MT
----- Original Message -----
From: AA0ZZ
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, January 07, 2012 2:55 PM
Subject: [PPLL-VFO] Re: CW Transmitter Circuit

Hi Justin,

Interesting question. It's time for an update / discussion about that circuit anyway.

No, you won't find this circuit elsewhere; it is a creation of mine, but it is based on ideas from many sources.

I would suggest that you pick up the latest version (v2b) of the transmitter - now in the FILES section and on my web page. While the original circuit probably works, it has some flaws in the divide-by-4 portion that should be corrected.

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centered signal is fed to the other XOR gate (U9a) and now a very small voltage swing will activate it. Now our 1.5v p-p signal will work it very nicely. R51, the 5.1k resistor, keeps the gate input offset a bit away from the center so that the gate will not oscillate. Different values can be used for R51, depending on how much sensivity is needed.

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By the way, the same XOR switching scheme should be used for the receivers that are driven by the Si570 and the divide-by-4 mechanism. I haven't updated all of the diagrams yet.

Let me know if you have questions.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "justinpinnix" <justin.pinnix@...> wrote:
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> Hi Folks,
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Is it based on a circuit from somewhere else that I can read up on? How much
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circuit band-specific?
>
> 73 de AJ4MJ
>

188. Encoder

Yahoo group: PPLL-VFO
Date: 2012-01-25 14:47:57 UTC
From: sa5bxt
Topic: 188 Message: 188

Hi
I planning to build this unit to use as a stand alone VFO for my QRP experiments. I´m going to buy the daughterbord as kit from Kangaus. As I look at komponent list I see that I most components needed, exept for the encoder. My question is what type it is, find that there are some different kind of encorders.. I realy looking forward to get this litle thing working, it seem´s fullfilmy needs completly!
73 de
SA5BXT
Mats

189. Re: Encoder

Yahoo group: PPLL-VFO
Date: 2012-01-25 20:53:42 UTC
From: Bill Oelker
Topic: 188 Message: 189

Hi Mats, Why don't you email Bill Kelsey at (Kangus.com) and ask him for a part number, he supplies those and the parts break down list shows Kanga also. He will surely point you in the correct direction.
Good Luck with your project, Bill KN8DMK..

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
>
> Hi
> I planning to build this unit to use as a stand alone VFO for my QRP experiments. I´m going to buy the daughterbord as kit from Kangaus. As I look at komponent list I see that I most components needed, exept for the encoder. My question is what type it is, find that there are some different kind of encorders.. I realy looking forward to get this litle thing working, it seem´s fullfilmy needs completly!
> 73 de
> SA5BXT
> Mats
>

190. Re: [PPLL-VFO] Encoder

Yahoo group: PPLL-VFO
Date: 2012-01-26 03:35:28 UTC
From: Craig Johnson, AA0ZZ
Topic: 188 Message: 190

Hi Mats,

Any encoder that puts out quadrature signals will work. In fact, it can be an optical encoder (there is +5v on one of the pins of
the header) or a mechanical encoder. Optical encoders are the generally best but they are very expensive (somewhere around $35) so,
at least while experimenting, mechanical encoders are more practical. Optical encoders put out more pulses per revolution, are very
smooth, and have the least "backlash" when changing direction.

Some mechanical encoders are very inexpensive (around $3 - $5 or so) but many are not particularly fun to use since they don't feel
good. The mechanical encoder that we use in the kit is a particularly good one - the best that I have ever seen in fact, but still
with a reasonable cost - so I am very happy to be able to offer it . This encoder is made in China and they must be purchased in
large quantities so they cannot be ordered by individuals.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Wednesday, January 25, 2012 8:47 AM
Subject: [PPLL-VFO] Encoder

> Hi
> I planning to build this unit to use as a stand alone VFO for my QRP experiments. I?m going to buy the daughterbord as kit from
> Kangaus. As I look at komponent list I see that I most components needed, exept for the encoder. My question is what type it is,
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> 73 de
> SA5BXT
> Mats
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> Yahoo! Groups Links
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191. Re: Encoder

Yahoo group: PPLL-VFO
Date: 2012-01-26 16:47:11 UTC
From: sa5bxt
Topic: 188 Message: 191

Hi
After some discusion (with myself...), I decide to buy a complete kit from kangaus. It´s probably the best way to get all parts I need!

Mats

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
>
> Hi
> I planning to build this unit to use as a stand alone VFO for my QRP experiments. I´m going to buy the daughterbord as kit from Kangaus. As I look at komponent list I see that I most components needed, exept for the encoder. My question is what type it is, find that there are some different kind of encorders.. I realy looking forward to get this litle thing working, it seem´s fullfilmy needs completly!
> 73 de
> SA5BXT
> Mats
>

192. Re: [PPLL-VFO] Re: Encoder

Yahoo group: PPLL-VFO
Date: 2012-01-26 18:07:11 UTC
From: Justin Pinnix
Topic: 188 Message: 192

It's a quick build - about an hour. I've built two (since I blew up the
first one :O).

72 de AJ4MJ

On Thu, Jan 26, 2012 at 11:47 AM, sa5bxt <mats.su@...> wrote:

> **
>
>
> Hi
> After some discusion (with myself...), I decide to buy a complete kit from
> kangaus. It´s probably the best way to get all parts I need!
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> Mats
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> > > 73 de
> > > SA5BXT
> > > Mats
> > >
>
>
>

193. Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 12:46:17 UTC
From: sa5bxt
Topic: 193 Message: 193

Hi!
Just finished my daughterboard. Voltages is ok, but default frequency is only 7.2Mhz. Have I blown the si570? It´s a bit problem to solder possible to much heat?

73 de SA5BXT Mats

194. Re: [PPLL-VFO] Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 14:16:25 UTC
From: Craig Johnson, AA0ZZ
Topic: 193 Message: 194

Hi Mats,

That is very strange - something I have not heard of before.
In fact, according to the spec sheet the Si570 is not supposed to be able to run below 10 MHz.
We all know it will work lower than 10 MHz but 7.2 MHz is a long way from 10 MHz.

Tell me more about your setup. Are you running the daughtercard in a PIC-EL board? If not, what
control board are you using?

As for software, is it the original PEGen570 software preprogrammed on a16F88 PIC or did you
make your own?

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, February 19, 2012 6:46 AM
Subject: [PPLL-VFO] Default freqency

> Hi!
> Just finished my daughterboard. Voltages is ok, but default frequency is only 7.2Mhz. Have I blown the si570? It?s a bit problem
> to solder possible to much heat?
>
> 73 de SA5BXT Mats
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
>
>
>
>

195. Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 17:07:07 UTC
From: sa5bxt
Topic: 193 Message: 195

Hi
I´m running the daughterbord "stand alone". Measure on pin 6 HDR1 back to Si570 pin 4. have used two different counters. 3.3V is present on pins 6 and 3 takes about 75ma complete card. Do I need to have the controlboard connected? Just finished the daughterboard, controlboard waiting to be completed.

73 de
Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mats,
>
> That is very strange - something I have not heard of before.
> In fact, according to the spec sheet the Si570 is not supposed to be able to run below 10 MHz.
> We all know it will work lower than 10 MHz but 7.2 MHz is a long way from 10 MHz.
>
> Tell me more about your setup. Are you running the daughtercard in a PIC-EL board? If not, what
> control board are you using?
>
> As for software, is it the original PEGen570 software preprogrammed on a16F88 PIC or did you
> make your own?
>
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Sunday, February 19, 2012 6:46 AM
> Subject: [PPLL-VFO] Default freqency
>
>
> > Hi!
> > Just finished my daughterboard. Voltages is ok, but default frequency is only 7.2Mhz. Have I blown the si570? It´s a bit problem
> > to solder possible to much heat?
> >
> > 73 de SA5BXT Mats
> >
> >
> >

> > ------------------------------------
> >
> > Yahoo! Groups Links
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196. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 22:03:08 UTC
From: Craig Johnson, AA0ZZ
Topic: 193 Message: 196

Mats,
It should come up at 10 MHz by itself. If you have the control board almost ready, it will be interesting
to see what it does with the software driving it.

Please look at the number printed on the top of the SI570. There should be no Si570 that ever runs that
low in frequency, let alone as the default.

73,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, February 19, 2012 11:07 AM
Subject: [PPLL-VFO] Re: Default freqency

> Hi
> I?m running the daughterbord "stand alone". Measure on pin 6 HDR1 back to Si570 pin 4. have used two different counters. 3.3V is
> present on pins 6 and 3 takes about 75ma complete card. Do I need to have the controlboard connected? Just finished the
> daughterboard, controlboard waiting to be completed.
>
> 73 de
> Mats
>
> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>>
>> Hi Mats,
>>
>> That is very strange - something I have not heard of before.
>> In fact, according to the spec sheet the Si570 is not supposed to be able to run below 10 MHz.
>> We all know it will work lower than 10 MHz but 7.2 MHz is a long way from 10 MHz.
>>
>> Tell me more about your setup. Are you running the daughtercard in a PIC-EL board? If not, what
>> control board are you using?
>>
>> As for software, is it the original PEGen570 software preprogrammed on a16F88 PIC or did you
>> make your own?
>>
>> Best Regards,

>> -Craig, AA0ZZ
>>
>> ----- Original Message -----
>> From: "sa5bxt" <mats.su@...>
>> To: <PPLL-VFO@yahoogroups.com>
>> Sent: Sunday, February 19, 2012 6:46 AM
>> Subject: [PPLL-VFO] Default freqency
>>
>>
>> > Hi!
>> > Just finished my daughterboard. Voltages is ok, but default frequency is only 7.2Mhz. Have I blown the si570? It?s a bit
>> > problem
>> > to solder possible to much heat?
>> >
>> > 73 de SA5BXT Mats
>> >
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> Yahoo! Groups Links
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197. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 22:24:12 UTC
From: richard
Topic: 193 Message: 197

On Sun, 19 Feb 2012 16:03:08 -0600
"Craig Johnson, AA0ZZ" <aa0zz@...> wrote:

> Mats,
> It should come up at 10 MHz by itself. If you have the control
> board almost ready, it will be interesting to see what it does with
> the software driving it.
>
> Please look at the number printed on the top of the SI570. There
> should be no Si570 that ever runs that low in frequency, let alone as
> the default.
>
> 73,
> -Craig, AA0ZZ
>long shot Mats, you have checked the voltages on the tracks and
possibly on the pads of the chip.
Check you have the ground connected to the chip, do a continuity check
between 0V ground and the case of the chip and the ground connection on
the chip,
Some devices will do some very strange things with a virtual ground,
the Si570 may be one, as I said a long shot.

--

--
Best wishes / 73
Richard Bown

e-mail: richard@... or richard.bown@...

nil carborundum a illegitemis
##
Ham Call G8JVM . OS Fedora FC16 x86_64 on a Dell Insiron N5030 laptop
Maidenhead QRA: IO82SP38, LAT. 52 39.720' N LONG. 2 28.171 W (degs
mins) QRV HF + VHF Microwave 23 cms:140W,13 cms:100W,6 cms:10W & 3
cms:5W
##

198. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-19 22:40:48 UTC
From: Stephen Farthing
Topic: 193 Message: 198

Hi Guys,

FYI the start up frequency of the Si570 may not always be 10 MHz....

http://dspradio.org/df7tv/src11 tells you of one which has 56.32 MHz and other frequencies.

73s Steve G0XAR

--
Wisdom demands a new orientation of science and technology towards the organic, the gentle, the non-violent, the elegant and beautiful. E. F. Schumacher

199. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 02:46:34 UTC
From: Craig Johnson, AA0ZZ
Topic: 193 Message: 199

The ones shipped with the daughtercards from Kanga are all 10 MHz. That's why I asked about the number on the top of the Si570 - in case a wrong one got mixed in.
Nevertheless, there is no part number for an Si570 that would start at 7.2 MHz.
Best Regards,
-Craig, AA0ZZ
----- Original Message -----
From: Stephen Farthing
To: PPLL-VFO@yahoogroups.com
Sent: Sunday, February 19, 2012 4:40 PM
Subject: Re: [PPLL-VFO] Re: Default freqency

Hi Guys,

FYI the start up frequency of the Si570 may not always be 10 MHz....

http://dspradio.org/df7tv/src11 tells you of one which has 56.32 MHz and other frequencies.

73s Steve G0XAR

--

Wisdom demands a new orientation of science and technology towards the organic, the gentle, the non-violent, the elegant and beautiful. E. F. Schumacher

200. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 08:00:49 UTC
From: Stephen Farthing
Topic: 193 Message: 200

Craig,

Sorry, I did not realise that you only ship 10 MHz parts.

I wonder if the 7.2 MHz is interference from the 40 Meter band and that the Si570 is not working. I know from personal experience that soldering the Si570 can be a bit tricky until you get the hang of it.

73s Steve G0XAR

--
Wisdom demands a new orientation of science and technology towards the organic, the gentle, the non-violent, the elegant and beautiful. E. F. Schumacher

201. Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 17:37:46 UTC
From: sa5bxt
Topic: 193 Message: 201

It´s embarrassing, bad soldering...Well some 40+ years with electronics does not seem to be enough when it comes to SMD! Thanks for all respons to my emergency call. My counter shows 9.99999 and so on Mhz. My scope is only up to 10Mhz (Hardly!)om mesurments is not so reliabel, but i looks like sinus curve som 3 V p-p is that ok?
73 de Mats

--- In PPLL-VFO@...m, Stephen Farthing <squirrox@...> wrote:
>
> Craig,
>
> Sorry, I did not realise that you only ship 10 MHz parts.
>
> I wonder if the 7.2 MHz is interference from the 40 Meter band and that
> the Si570 is not working. I know from personal experience that soldering
> the Si570 can be a bit tricky until you get the hang of it.
>
> 73s Steve G0XAR
>
> --
> Wisdom demands a new orientation of science and technology towards the
> organic, the gentle, the non-violent, the elegant and beautiful. E. F.
> Schumacher
>

202. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 17:42:52 UTC
From: Bob Macklin
Topic: 193 Message: 202

Where do people buy their Si 570s?

I got a couple a few years ago but it was difficult. The common distributors do not stock them.

Bob K5MYJ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, February 20, 2012 9:37 AM
Subject: [PPLL-VFO] Re: Default freqency

It?s embarrassing, bad soldering...Well some 40+ years with electronics does not seem to be enough when it comes to SMD! Thanks for all respons to my emergency call. My counter shows 9.99999 and so on Mhz. My scope is only up to 10Mhz (Hardly!)om mesurments is not so reliabel, but i looks like sinus curve som 3 V p-p is that ok?
73 de Mats

--- In PPLL-VFO@yahoogroups.com, Stephen Farthing <squirrox@...> wrote:
>
> Craig,
>
> Sorry, I did not realise that you only ship 10 MHz parts.
>
> I wonder if the 7.2 MHz is interference from the 40 Meter band and that
> the Si570 is not working. I know from personal experience that soldering
> the Si570 can be a bit tricky until you get the hang of it.
>
> 73s Steve G0XAR
>
> --
> Wisdom demands a new orientation of science and technology towards the
> organic, the gentle, the non-violent, the elegant and beautiful. E. F.
> Schumacher
>

Yahoo! Groups Links

203. Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 17:46:46 UTC
From: Stephen Farthing
Topic: 193 Message: 203

They are actually quite difficult to solder.....they can look soldered....but sometimes the contact is not so good....I took 3 goes to solder my first one....

--
Wisdom demands a new orientation of science and technology towards the organic, the gentle, the non-violent, the elegant and beautiful. E. F. Schumacher

204. Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 18:03:24 UTC
From: sa5bxt
Topic: 193 Message: 204

Thanks to hear Stephen, i´m not the first and probably not the last....
Mats

--- In PPLL-VFO@yahoogroups.com, Stephen Farthing <squirrox@...> wrote:
>
> They are actually quite difficult to solder.....they can look
> soldered....but sometimes the contact is not so good....I took 3 goes to
> solder my first one....
>
> --
> Wisdom demands a new orientation of science and technology towards the
> organic, the gentle, the non-violent, the elegant and beautiful. E. F.
> Schumacher
>

205. Test!

Yahoo group: PPLL-VFO
Date: 2012-02-20 18:51:46 UTC
From: Bob Macklin
Topic: 205 Message: 205

Just an email change test!

Bob K5MYJ

206. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 22:01:20 UTC
From: Craig Johnson, AA0ZZ
Topic: 193 Message: 206

Bob,

It is best to order them directly from Silicon Labs. Mouser stocked a few types but it's difficult to
make sure you getting exactly what you want. I've found discrepancies between what their catalog
descriptions and the part numbers. All I can say is to be careful if you try to order these from Mouser.

When ordering from Silicon Labs there is quite a long lead time (2-4 weeks) on the parts since they
are "programmed to order" for the frequency that you select via the part number.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "Bob Macklin" <macklinbob@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, February 20, 2012 11:42 AM
Subject: Re: [PPLL-VFO] Re: Default freqency

> Where do people buy their Si 570s?
>
> I got a couple a few years ago but it was difficult. The common distributors
> do not stock them.
>
> Bob K5MYJ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Monday, February 20, 2012 9:37 AM
> Subject: [PPLL-VFO] Re: Default freqency
>
>
> It?s embarrassing, bad soldering...Well some 40+ years with electronics does
> not seem to be enough when it comes to SMD! Thanks for all respons to my
> emergency call. My counter shows 9.99999 and so on Mhz. My scope is only up
> to 10Mhz (Hardly!)om mesurments is not so reliabel, but i looks like sinus
> curve som 3 V p-p is that ok?
> 73 de Mats
>
> --- In PPLL-VFO@yahoogroups.com, Stephen Farthing <squirrox@...> wrote:
>>
>> Craig,

>>
>> Sorry, I did not realise that you only ship 10 MHz parts.
>>
>> I wonder if the 7.2 MHz is interference from the 40 Meter band and that
>> the Si570 is not working. I know from personal experience that soldering
>> the Si570 can be a bit tricky until you get the hang of it.
>>
>> 73s Steve G0XAR
>>
>> --
>> Wisdom demands a new orientation of science and technology towards the
>> organic, the gentle, the non-violent, the elegant and beautiful. E. F.
>> Schumacher
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> Yahoo! Groups Links
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> Yahoo! Groups Links
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207. Re: [PPLL-VFO] Re: Default freqency

Yahoo group: PPLL-VFO
Date: 2012-02-20 22:09:14 UTC
From: Craig Johnson, AA0ZZ
Topic: 193 Message: 207

Mats,
Great! Glad you were able to get it working.

Yes, we've all had soldering issues from time to time. These parts are not as small as the pins of a DDS but
you do have to be careful. These can be soldered without a microscope but good light and some sort of
magnification sure helps.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, February 20, 2012 11:37 AM
Subject: [PPLL-VFO] Re: Default freqency

> It?s embarrassing, bad soldering...Well some 40+ years with electronics does not seem to be enough when it comes to SMD! Thanks
> for all respons to my emergency call. My counter shows 9.99999 and so on Mhz. My scope is only up to 10Mhz (Hardly!)om mesurments
> is not so reliabel, but i looks like sinus curve som 3 V p-p is that ok?
> 73 de Mats
>
> --- In PPLL-VFO@yahoogroups.com, Stephen Farthing <squirrox@...> wrote:
>>
>> Craig,
>>
>> Sorry, I did not realise that you only ship 10 MHz parts.
>>
>> I wonder if the 7.2 MHz is interference from the 40 Meter band and that
>> the Si570 is not working. I know from personal experience that soldering
>> the Si570 can be a bit tricky until you get the hang of it.
>>
>> 73s Steve G0XAR
>>
>> --
>> Wisdom demands a new orientation of science and technology towards the
>> organic, the gentle, the non-violent, the elegant and beautiful. E. F.
>> Schumacher
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> Yahoo! Groups Links
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208. Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-22 11:23:13 UTC
From: sa5bxt
Topic: 208 Message: 208

Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do I do to get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the "learning by doing" and "trial and error" methods in my way to become aham radio amateur.
73 de
Mats

209. Re: [PPLL-VFO] Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-23 00:42:12 UTC
From: Craig Johnson, AA0ZZ
Topic: 208 Message: 209

Mats,

Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
Si570 CW Transmitter.

By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
1.5v signal "more robust" and then it will meet the spec requirements. Look back at message number 184 and see more details of how the "Exclusive ORs" work in this circuit.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Wednesday, February 22, 2012 5:23 AM
Subject: [PPLL-VFO] Lower bands

> Well, here I am again! My project run?s perfect. But, as a beginner in higher frequency, a new question pop?s up. how do I do to
> get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I?m using the "learning by doing"
> and "trial and error" methods in my way to become aham radio amateur.
> 73 de
> Mats
>
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> ------------------------------------
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> Yahoo! Groups Links
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210. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-23 19:04:57 UTC
From: sa5bxt
Topic: 208 Message: 210

Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?

Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Mats,
>
> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
> Si570 CW Transmitter.
>
> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
> quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
>
> Best Regards,
> -Craig, AA0ZZ
>
>
>
>
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@...m>
> Sent: Wednesday, February 22, 2012 5:23 AM
> Subject: [PPLL-VFO] Lower bands
>
>
> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do I do to
> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you

can see I´m using the "learning by doing"
> > and "trial and error" methods in my way to become aham radio amateur.
> > 73 de
> > Mats
> >
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> > Yahoo! Groups Links
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>

211. Re: [PPLL-VFO] Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-24 12:50:23 UTC
From: Craig Johnson, AA0ZZ
Topic: 208 Message: 211

Mats,
What you need following the flip-flops depends on what you want to do with the signal.
It is a square wave at that point.
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Thursday, February 23, 2012 1:04 PM
Subject: [PPLL-VFO] Re: Lower bands

> Thanks! I guess it must be fast 74-circuits so?I must do some shopping. Do I need some buffer on the output?
>
> Mats
>
> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>>
>> Mats,
>>
>> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
>> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
>> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
>> Si570 CW Transmitter.
>>
>> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
>> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
>> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
>> quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
>> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
>> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
>>
>> Best Regards,
>> -Craig, AA0ZZ
>>
>>
>>

>>
>>
>> ----- Original Message -----
>> From: "sa5bxt" <mats.su@...>
>> To: <PPLL-VFO@yahoogroups.com>
>> Sent: Wednesday, February 22, 2012 5:23 AM
>> Subject: [PPLL-VFO] Lower bands
>>
>>
>> > Well, here I am again! My project run?s perfect. But, as a beginner in higher frequency, a new question pop?s up. how do I do
>> > to
>> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I?m using the "learning by doing"
>> > and "trial and error" methods in my way to become aham radio amateur.
>> > 73 de
>> > Mats
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212. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-26 15:31:57 UTC
From: sa5bxt
Topic: 208 Message: 212

Hi
While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
73 de
Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Mats,
> What you need following the flip-flops depends on what you want to do with the signal.
> It is a square wave at that point.
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@...m>
> Sent: Thursday, February 23, 2012 1:04 PM
> Subject: [PPLL-VFO] Re: Lower bands
>
>
> > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?
> >
> > Mats
> >
> > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >>
> >> Mats,
> >>
> >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
> >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> >> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
> >> Si570 CW Transmitter.
> >>
> >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
> >> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
> >> quite enough for every part in every situation. Using the two "Exclusive OR" gates in

front makes the
> >> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
> >> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
> >>
> >> Best Regards,
> >> -Craig, AA0ZZ
> >>
> >>
> >>
> >>
> >>
> >> ----- Original Message -----
> >> From: "sa5bxt" <mats.su@>
> >> To: <PPLL-VFO@yahoogroups.com>
> >> Sent: Wednesday, February 22, 2012 5:23 AM
> >> Subject: [PPLL-VFO] Lower bands
> >>
> >>
> >> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do I do
> >> > to
> >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the "learning by doing"
> >> > and "trial and error" methods in my way to become aham radio amateur.
> >> > 73 de
> >> > Mats
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213. Re: [PPLL-VFO] Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-26 16:17:22 UTC
From: Jim or Cathy Wallace
Topic: 208 Message: 213

Just from glancing at the data sheet, I suspect the answer is no. This part is intended for operation at 1 gHz. The graph of their operating "window" stops at 100 mHz, so you still might not get the range you want. Input levels run around 100 mV and output around 1 volt p-p, which might not be enough for what you want. But, you've got the part, so what's the harm in trying it out? Experiment.

Jim
KB5MT
----- Original Message -----
From: sa5bxt
To: PPLL-VFO@yahoogroups.com
Sent: Sunday, February 26, 2012 9:31 AM
Subject: [PPLL-VFO] Re: Lower bands

Hi
While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
73 de
Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Mats,
> What you need following the flip-flops depends on what you want to do with the signal.
> It is a square wave at that point.
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Thursday, February 23, 2012 1:04 PM
> Subject: [PPLL-VFO] Re: Lower bands
>
>
> > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?
> >
> > Mats
> >
> > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >>
> >> Mats,
> >>
> >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.

> >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> >> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
> >> Si570 CW Transmitter.
> >>
> >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
> >> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
> >> quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
> >> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
> >> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
> >>
> >> Best Regards,
> >> -Craig, AA0ZZ
> >>
> >>
> >>
> >>
> >>
> >> ----- Original Message -----
> >> From: "sa5bxt" <mats.su@>
> >> To: <PPLL-VFO@yahoogroups.com>
> >> Sent: Wednesday, February 22, 2012 5:23 AM
> >> Subject: [PPLL-VFO] Lower bands
> >>
> >>
> >> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do I do
> >> > to
> >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the "learning by doing"
> >> > and "trial and error" methods in my way to become aham radio amateur.
> >> > 73 de
> >> > Mats
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214. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-26 21:10:15 UTC
From: sa5bxt
Topic: 208 Message: 214

I agree, but I don´t think the frequency is the problem. It´s only dived by 10, so that probably leeds to new software, and much of the quality of Si project is gone (I think!). So I work´s on with my 74 logic that been proven work perfect. But some brainstorming is never wrong for creativity!
73 de
Mats

--- In PPLL-VFO@yahoogroups.com, "Jim or Cathy Wallace" <jimandcathywallace@...> wrote:
>
> Just from glancing at the data sheet, I suspect the answer is no. This part is intended for operation at 1 gHz. The graph of their operating "window" stops at 100 mHz, so you still might not get the range you want. Input levels run around 100 mV and output around 1 volt p-p, which might not be enough for what you want. But, you've got the part, so what's the harm in trying it out? Experiment.
>
> Jim
> KB5MT
> ----- Original Message -----
> From: sa5bxt
> To: PPLL-VFO@yahoogroups.com
> Sent: Sunday, February 26, 2012 9:31 AM
> Subject: [PPLL-VFO] Re: Lower bands
>
>
>
> Hi
> While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
> 73 de
> Mats
>
> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >
> > Mats,
> > What you need following the flip-flops depends on what you want to do with the signal.
> > It is a square wave at that point.
> > Best Regards,
> > -Craig, AA0ZZ
> >
> > ----- Original Message -----
> > From: "sa5bxt" <mats.su@>
> > To: <PPLL-VFO@yahoogroups.com>
> > Sent: Thursday, February 23, 2012 1:04 PM
> > Subject: [PPLL-VFO] Re: Lower bands

> >
> >
> > > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?
> > >
> > > Mats
> > >
> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> > >>
> > >> Mats,
> > >>
> > >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
> > >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> > >> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
> > >> Si570 CW Transmitter.
> > >>
> > >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> > >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
> > >> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
> > >> quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
> > >> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
> > >> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
> > >>
> > >> Best Regards,
> > >> -Craig, AA0ZZ
> > >>
> > >>
> > >>
> > >>
> > >>
> > >>
> > >> ----- Original Message -----
> > >> From: "sa5bxt" <mats.su@>
> > >> To: <PPLL-VFO@yahoogroups.com>
> > >> Sent: Wednesday, February 22, 2012 5:23 AM
> > >> Subject: [PPLL-VFO] Lower bands
> > >>
> > >>
> > >> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do I do
> > >> > to
> > >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the "learning by doing"
> > >> > and "trial and error" methods in my way to become aham radio amateur.

> > >> > 73 de
> > >> > Mats
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215. Re: [PPLL-VFO] Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-02-26 23:25:22 UTC
From: Craig Johnson, AA0ZZ
Topic: 208 Message: 215

Mats,

Yes, it's always interesting to try things.

Getting the software to run with your new division factor is another issue. Of course changes could be made to the software to
display the correct frequency, since "it's just code". The source code is there but it would take a considerable amount
of work. The current display routine just divides the frequency by 2 or 4 (if the "divide-by-x" flag is set) by simply shifting the
Si570 frequency by 1or 2. The new display routine would need a much more complicated algorithm.
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, February 26, 2012 3:10 PM
Subject: [PPLL-VFO] Re: Lower bands

>I agree, but I don?t think the frequency is the problem. It?s only dived by 10, so that probably leeds to new software, and much of
>the quality of Si project is gone (I think!). So I work?s on with my 74 logic that been proven work perfect. But some
>brainstorming is never wrong for creativity!
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> Mats
>
> --- In PPLL-VFO@yahoogroups.com, "Jim or Cathy Wallace" <jimandcathywallace@...> wrote:
>>
>> Just from glancing at the data sheet, I suspect the answer is no. This part is intended for operation at 1 gHz. The graph of
>> their operating "window" stops at 100 mHz, so you still might not get the range you want. Input levels run around 100 mV and
>> output around 1 volt p-p, which might not be enough for what you want. But, you've got the part, so what's the harm in trying it
>> out? Experiment.
>>
>> Jim
>> KB5MT
>> ----- Original Message -----
>> From: sa5bxt
>> To: PPLL-VFO@yahoogroups.com
>> Sent: Sunday, February 26, 2012 9:31 AM
>> Subject: [PPLL-VFO] Re: Lower bands

>>
>>
>>
>> Hi
>> While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in
>> another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
>> 73 de
>> Mats
>>
>> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
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>> > Mats,
>> > What you need following the flip-flops depends on what you want to do with the signal.
>> > It is a square wave at that point.
>> > Best Regards,
>> > -Craig, AA0ZZ
>> >
>> > ----- Original Message -----
>> > From: "sa5bxt" <mats.su@>
>> > To: <PPLL-VFO@yahoogroups.com>
>> > Sent: Thursday, February 23, 2012 1:04 PM
>> > Subject: [PPLL-VFO] Re: Lower bands
>> >
>> >
>> > > Thanks! I guess it must be fast 74-circuits so?I must do some shopping. Do I need some buffer on the output?
>> > >
>> > > Mats
>> > >
>> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
>> > >>
>> > >> Mats,
>> > >>
>> > >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
>> > >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
>> > >> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
>> > >> Si570 CW Transmitter.
>> > >>
>> > >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
>> > >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
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>> > >> quite enough for every part in every situation. Using the two "Exclusive OR" gates

in front makes the
>> > >> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
>> > >> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
>> > >>
>> > >> Best Regards,
>> > >> -Craig, AA0ZZ
>> > >>
>> > >>
>> > >>
>> > >>
>> > >>
>> > >> ----- Original Message -----
>> > >> From: "sa5bxt" <mats.su@>
>> > >> To: <PPLL-VFO@yahoogroups.com>
>> > >> Sent: Wednesday, February 22, 2012 5:23 AM
>> > >> Subject: [PPLL-VFO] Lower bands
>> > >>
>> > >>
>> > >> > Well, here I am again! My project run?s perfect. But, as a beginner in higher frequency, a new question pop?s up. how do
>> I do
>> > >> > to
>> > >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I?m using the "learning by
>> doing"
>> > >> > and "trial and error" methods in my way to become aham radio amateur.
>> > >> > 73 de
>> > >> > Mats
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216. New file uploaded to PPLL-VFO

Yahoo group: PPLL-VFO
Date: 2012-03-03 17:12:45 UTC
From: PPLL-VFO@yahoogroups.com
Topic: 216 Message: 216

Hello,

This email message is a notification to let you know that
a file has been uploaded to the Files area of the PPLL-VFO
group.

File : /QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch
Uploaded by : jimhwallace <jimandcathywallace@...>
Description :

You can access this file at the URL:
http://groups.yahoo.com/group/PPLL-VFO/files/QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch

To learn more about file sharing for your group, please visit:
http://help.yahoo.com/l/us/yahoo/groups/original/members/web/index.html
Regards,

jimhwallace <jimandcathywallace@...>

217. Quadrature-detector receiver for Si570

Yahoo group: PPLL-VFO
Date: 2012-03-03 17:23:54 UTC
From: Jim or Cathy Wallace
Topic: 217 Message: 217

I got an enquiry this morning, so rather than delay even more, I've posted what I've got, so far, on boards for a quadrature-detector receiver based on the MicroR2 receiver, using the Si570 oscillator. I have NOT actually made this radio, yet, so everything is subject to change.

The PDF files are made from scans of printouts. The technical files for DIP TRACE are included. DCH files are schematics, DIP files are layouts. Look at the MS Word file for more explanation. a link for DIP TRACE software is included. FYI, it works pretty well.

I'll update and provide more information as I proceed, but please realize, it's spring here. The water is calling and there's work to be done. As someone said, life gets in the way.

Jim
KB5MT

218. Re: [PPLL-VFO] New file uploaded to PPLL-VFO

Yahoo group: PPLL-VFO
Date: 2012-03-03 23:47:01 UTC
From: Zack Widup
Topic: 216 Message: 218

What is a .dch file? I can't open it.

73, Zack W9SZ

On Sat, Mar 3, 2012 at 11:12 AM, <PPLL-VFO@yahoogroups.com> wrote:

>
> Hello,
>
> This email message is a notification to let you know that
> a file has been uploaded to the Files area of the PPLL-VFO
> group.
>
> File : /QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch
> Uploaded by : jimhwallace <jimandcathywallace@...>
> Description :
>
> You can access this file at the URL:
>
> http://groups.yahoo.com/group/PPLL-VFO/files/QuadradureDetectorRcvr/MicroR2FrontEndSWITC
H.dch
>
> To learn more about file sharing for your group, please visit:
> http://help.yahoo.com/l/us/yahoo/groups/original/members/web/index.html
> Regards,
>
> jimhwallace <jimandcathywallace@...>
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> Yahoo! Groups Links
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219. Re: [PPLL-VFO] New file uploaded to PPLL-VFO

Yahoo group: PPLL-VFO
Date: 2012-03-04 00:40:57 UTC
From: Jim or Cathy Wallace
Topic: 216 Message: 219

The .dch and .dip files are native files for DIP TRACE. You must install that software to use these files. Sorry, it's not my rule. If you don't want to modify anything, I think you can get along without using them by using the pertinent .pdf files. Read the .doc file for details. If you opened that early this morning, check to see if you've got the latest version because I later corrected a couple of things and put in the link. If it doesn't work as a link (now that I think of it), you can at least copy and paste in your browser to get the software. That takes some learning and there's some frustration involved, but I found that it actually works pretty well when you figure out how to do things "its" way (as in all software, right?)

Jim
----- Original Message -----
From: Zack Widup
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, March 03, 2012 5:47 PM
Subject: Re: [PPLL-VFO] New file uploaded to PPLL-VFO

What is a .dch file? I can't open it.

73, Zack W9SZ

On Sat, Mar 3, 2012 at 11:12 AM, <PPLL-VFO@yahoogroups.com> wrote:

Hello,

This email message is a notification to let you know that
a file has been uploaded to the Files area of the PPLL-VFO
group.

File : /QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch
Uploaded by : jimhwallace <jimandcathywallace@embarqmail.com>
Description :

You can access this file at the URL:
http://groups.yahoo.com/group/PPLL-VFO/files/QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch

To learn more about file sharing for your group, please visit:
http://help.yahoo.com/l/us/yahoo/groups/original/members/web/index.html
Regards,

jimhwallace <jimandcathywallace@embarqmail.com>

Yahoo! Groups Links

220. Re: [PPLL-VFO] New file uploaded to PPLL-VFO

Yahoo group: PPLL-VFO
Date: 2012-03-04 07:32:56 UTC
From: Zack Widup
Topic: 216 Message: 220

Thanks! I downloaded and installed the free version of DipTrace. Looks like
a cool program.

73, Zack W9SZ

On Sat, Mar 3, 2012 at 6:40 PM, Jim or Cathy Wallace <
jimandcathywallace@...> wrote:

> **
>
>
> The .dch and .dip files are native files for DIP TRACE. You must install
> that software to use these files. Sorry, it's not my rule. If you don't
> want to modify anything, I think you can get along without using them by
> using the pertinent .pdf files. Read the .doc file for details. If you
> opened that early this morning, check to see if you've got the latest
> version because I later corrected a couple of things and put in the link.
> If it doesn't work as a link (now that I think of it), you can at least
> copy and paste in your browser to get the software. That takes some
> learning and there's some frustration involved, but I found that it
> actually works pretty well when you figure out how to do things "its" way
> (as in all software, right?)
>
> Jim
>
> ----- Original Message -----
> *From:* Zack Widup <w9sz.zack@...>
> *To:* PPLL-VFO@yahoogroups.com
> *Sent:* Saturday, March 03, 2012 5:47 PM
> *Subject:* Re: [PPLL-VFO] New file uploaded to PPLL-VFO
>
>
>
>
> What is a .dch file? I can't open it.
>
> 73, Zack W9SZ
>
>
> On Sat, Mar 3, 2012 at 11:12 AM, <PPLL-VFO@yahoogroups.com> wrote:
>
>>
>> Hello,
>>
>> This email message is a notification to let you know that
>> a file has been uploaded to the Files area of the PPLL-VFO
>> group.

>>
>> File : /QuadradureDetectorRcvr/MicroR2FrontEndSWITCH.dch
>> Uploaded by : jimhwallace <jimandcathywallace@...>
>> Description :
>>
>> You can access this file at the URL:
>>
>> http://groups.yahoo.com/group/PPLL-VFO/files/QuadradureDetectorRcvr/MicroR2FrontEndSWIT
CH.dch
>>
>> To learn more about file sharing for your group, please visit:
>> http://help.yahoo.com/l/us/yahoo/groups/original/members/web/index.html
>> Regards,
>>
>> jimhwallace <jimandcathywallace@...>
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221. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-10 17:16:07 UTC
From: sa5bxt
Topic: 208 Message: 221

My divide by 4 works nice, but it stops round 14MHz. Is this due to 74 logic? I´m using HC and AC. Another question is if RF output could go direct to VFO input at my SSB transciver? Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Mats,
>
> Yes, it's always interesting to try things.
>
> Getting the software to run with your new division factor is another issue. Of course changes could be made to the software to
> display the correct frequency, since "it's just code". The source code is there but it would take a considerable amount
> of work. The current display routine just divides the frequency by 2 or 4 (if the "divide-by-x" flag is set) by simply shifting the
> Si570 frequency by 1or 2. The new display routine would need a much more complicated algorithm.
> Best Regards,
> -Craig, AA0ZZ
>
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Sunday, February 26, 2012 3:10 PM
> Subject: [PPLL-VFO] Re: Lower bands
>
>
> >I agree, but I don´t think the frequency is the problem. It´s only dived by 10, so that probably leeds to new software, and much of
> >the quality of Si project is gone (I think!). So I work´s on with my 74 logic that been proven work perfect. But some
> >brainstorming is never wrong for creativity!
> > 73 de
> > Mats
> >
> > --- In PPLL-VFO@yahoogroups.com, "Jim or Cathy Wallace" <jimandcathywallace@> wrote:
> >>
> >> Just from glancing at the data sheet, I suspect the answer is no. This part is intended for operation at 1 gHz. The graph of
> >> their operating "window" stops at 100 mHz, so you still might not get the range you want. Input levels run around 100 mV and
> >> output around 1 volt p-p, which might not be enough for what you want. But, you've got the part, so what's the harm in trying it

> >> out? Experiment.
> >>
> >> Jim
> >> KB5MT
> >> ----- Original Message -----
> >> From: sa5bxt
> >> To: PPLL-VFO@yahoogroups.com
> >> Sent: Sunday, February 26, 2012 9:31 AM
> >> Subject: [PPLL-VFO] Re: Lower bands
> >>
> >>
> >>
> >> Hi
> >> While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in
> >> another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
> >> 73 de
> >> Mats
> >>
> >> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >> >
> >> > Mats,
> >> > What you need following the flip-flops depends on what you want to do with the signal.
> >> > It is a square wave at that point.
> >> > Best Regards,
> >> > -Craig, AA0ZZ
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> >> > ----- Original Message -----
> >> > From: "sa5bxt" <mats.su@>
> >> > To: <PPLL-VFO@yahoogroups.com>
> >> > Sent: Thursday, February 23, 2012 1:04 PM
> >> > Subject: [PPLL-VFO] Re: Lower bands
> >> >
> >> >
> >> > > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?
> >> > >
> >> > > Mats
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> >> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >> > >>
> >> > >> Mats,
> >> > >>
> >> > >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
> >> > >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> >> > >> sample designs in the FILES section. For a starter, see the mechanism in the

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> >> > >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> >> > >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
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> >> > >> Best Regards,
> >> > >> -Craig, AA0ZZ
> >> > >>
> >> > >>
> >> > >>
> >> > >>
> >> > >>
> >> > >> ----- Original Message -----
> >> > >> From: "sa5bxt" <mats.su@>
> >> > >> To: <PPLL-VFO@yahoogroups.com>
> >> > >> Sent: Wednesday, February 22, 2012 5:23 AM
> >> > >> Subject: [PPLL-VFO] Lower bands
> >> > >>
> >> > >>
> >> > >> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up. how do
> >> I do
> >> > >> > to
> >> > >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the "learning by
> >> doing"
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> >> > >> > 73 de
> >> > >> > Mats
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222. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-10 17:50:32 UTC
From: AA0ZZ
Topic: 208 Message: 222

Mats,

Don't know. As I recall, mine works up to at least 28 MHz .

Did you include the "exclusive-or" circuitry in front of the flip-flops? This will make the driving signal from the SI570 a little more robust.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
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> My divide by 4 works nice, but it stops round 14MHz. Is this due to 74 logic? I´m using HC and AC. Another question is if RF output could go direct to VFO input at my SSB transciver?
> Mats
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> > Yes, it's always interesting to try things.
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> > Getting the software to run with your new division factor is another issue. Of course changes could be made to the software to
> > display the correct frequency, since "it's just code". The source code is there but it would take a considerable amount
> > of work. The current display routine just divides the frequency by 2 or 4 (if the "divide-by-x" flag is set) by simply shifting the
> > Si570 frequency by 1or 2. The new display routine would need a much more complicated algorithm.
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> > ----- Original Message -----
> > From: "sa5bxt" <mats.su@>
> > To: <PPLL-VFO@yahoogroups.com>
> > Sent: Sunday, February 26, 2012 3:10 PM
> > Subject: [PPLL-VFO] Re: Lower bands
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> >
> > >I agree, but I don´t think the frequency is the problem. It´s only dived by 10, so that probably leeds to new software, and much of
> > >the quality of Si project is gone (I think!). So I work´s on with my 74 logic that been proven work perfect. But some

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> > >> their operating "window" stops at 100 mHz, so you still might not get the range you want. Input levels run around 100 mV and
> > >> output around 1 volt p-p, which might not be enough for what you want. But, you've got the part, so what's the harm in trying it
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> > >> Jim
> > >> KB5MT
> > >> ----- Original Message -----
> > >> From: sa5bxt
> > >> To: PPLL-VFO@yahoogroups.com
> > >> Sent: Sunday, February 26, 2012 9:31 AM
> > >> Subject: [PPLL-VFO] Re: Lower bands
> > >>
> > >>
> > >>
> > >> Hi
> > >> While serching in my component boxes, I find a little prescaler circuit,MC12080. It divide by 10,20,40,80. It was used in
> > >> another VFO circuit i found on the net (Before I find the SI project!) Is it possible to use that to get lower frequency?
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> > >> > What you need following the flip-flops depends on what you want to do with the signal.
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> > >> > From: "sa5bxt" <mats.su@>
> > >> > To: <PPLL-VFO@yahoogroups.com>
> > >> > Sent: Thursday, February 23, 2012 1:04 PM
> > >> > Subject: [PPLL-VFO] Re: Lower bands
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> > >> > > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?

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223. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-11 09:27:49 UTC
From: sa5bxt
Topic: 208 Message: 223

Hi!

I´m using first part of your 7MHz CW 74HC86 and 74AC74. Ouestion is if output is to low for my counter, it´s on the lowest sensitivity (15mVrms). I (Think) noticed lower sensitivity at higher freqency. Range is no problem it follows perfect when in divide by "1" mode. Do I need some kind of buffer amp after flip-flop?

Regards
Mats

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>
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> Don't know. As I recall, mine works up to at least 28 MHz .
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> > > From: "sa5bxt" <mats.su@>
> > > To: <PPLL-VFO@yahoogroups.com>
> > > Sent: Sunday, February 26, 2012 3:10 PM
> > > Subject: [PPLL-VFO] Re: Lower bands
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224. Re: [PPLL-VFO] Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-11 14:13:42 UTC
From: Craig Johnson, AA0ZZ
Topic: 208 Message: 224

Hi Mats,
I'm not sure what the problem is. You should have plenty of output from the flip-flops to measure in your counter.
You say "range is no problem and it follows perfectly when in divide by 1 mode". Does this mean that you can
look at the Si570 output (before it is divided) and you can count to higher frequencies? If so, it looks like the
XOR circuits or the flip flops are not keeping up. Strange.

Anyone else have any ideas?

-Craig

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, March 11, 2012 4:27 AM
Subject: [PPLL-VFO] Re: Lower bands

> Hi!
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> sensitivity (15mVrms). I (Think) noticed lower sensitivity at higher freqency. Range is no problem it follows perfect when in
> divide by "1" mode. Do I need some kind of buffer amp after flip-flop?
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>> Mats,
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>> Don't know. As I recall, mine works up to at least 28 MHz .
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>> Did you include the "exclusive-or" circuitry in front of the flip-flops? This will make the driving signal from the SI570 a
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>> > > >> > >> > and "trial and error" methods in my way to become aham radio amateur.
>> > > >> > >> > 73 de
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225. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-11 19:54:31 UTC
From: sa5bxt
Topic: 208 Message: 225

Hi Craig
This is a real mystery! XOR works all the way up in frequency, flip flop´s just to 13-14MHz. I test with a new 74ac74, all th same!

Regards
Mats

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mats,
> I'm not sure what the problem is. You should have plenty of output from the flip-flops to measure in your counter.
> You say "range is no problem and it follows perfectly when in divide by 1 mode". Does this mean that you can
> look at the Si570 output (before it is divided) and you can count to higher frequencies? If so, it looks like the
> XOR circuits or the flip flops are not keeping up. Strange.
>
> Anyone else have any ideas?
>
> -Craig
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Sunday, March 11, 2012 4:27 AM
> Subject: [PPLL-VFO] Re: Lower bands
>
>
> > Hi!
> >
> > I´m using first part of your 7MHz CW 74HC86 and 74AC74. Ouestion is if output is to low for my counter, it´s on the lowest
> > sensitivity (15mVrms). I (Think) noticed lower sensitivity at higher freqency. Range is no problem it follows perfect when in
> > divide by "1" mode. Do I need some kind of buffer amp after flip-flop?
> >
> > Regards
> > Mats
> >
> > --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> >>
> >> Mats,
> >>
> >> Don't know. As I recall, mine works up to at least 28 MHz .

> >>
> >> Did you include the "exclusive-or" circuitry in front of the flip-flops? This will make the driving signal from the SI570 a
> >> little more robust.
> >>
> >> Best Regards,
> >> -Craig, AA0ZZ
> >>
> >>
> >> --- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@> wrote:
> >> >
> >> > My divide by 4 works nice, but it stops round 14MHz. Is this due to 74 logic? I´m using HC and AC. Another question is if RF
> >> > output could go direct to VFO input at my SSB transciver?
> >> > Mats
> >> >
> >> > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
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> >> > > Mats,
> >> > >
> >> > > Yes, it's always interesting to try things.
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> >> > > Getting the software to run with your new division factor is another issue. Of course changes could be made to the software
> >> > > to
> >> > > display the correct frequency, since "it's just code". The source code is there but it would take a considerable amount
> >> > > of work. The current display routine just divides the frequency by 2 or 4 (if the "divide-by-x" flag is set) by simply
> >> > > shifting the
> >> > > Si570 frequency by 1or 2. The new display routine would need a much more complicated algorithm.
> >> > > Best Regards,
> >> > > -Craig, AA0ZZ
> >> > >
> >> > >
> >> > > ----- Original Message -----
> >> > > From: "sa5bxt" <mats.su@>
> >> > > To: <PPLL-VFO@yahoogroups.com>
> >> > > Sent: Sunday, February 26, 2012 3:10 PM
> >> > > Subject: [PPLL-VFO] Re: Lower bands
> >> > >
> >> > >
> >> > > >I agree, but I don´t think the frequency is the problem. It´s only dived by 10, so that probably leeds to new software, and
> >> > > >much of
> >> > > >the quality of Si project is gone (I think!). So I work´s on with my 74 logic that been proven work perfect. But some
> >> > > >brainstorming is never wrong for creativity!
> >> > > > 73 de

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> >> > > > --- In PPLL-VFO@yahoogroups.com, "Jim or Cathy Wallace" <jimandcathywallace@>
wrote:
> >> > > >>
> >> > > >> Just from glancing at the data sheet, I suspect the answer is no. This part is
intended for operation at 1 gHz. The
> >> > > >> graph of
> >> > > >> their operating "window" stops at 100 mHz, so you still might not get the range
you want. Input levels run around 100 mV
> >> > > >> and
> >> > > >> output around 1 volt p-p, which might not be enough for what you want. But,
you've got the part, so what's the harm in
> >> > > >> trying it
> >> > > >> out? Experiment.
> >> > > >>
> >> > > >> Jim
> >> > > >> KB5MT
> >> > > >> ----- Original Message -----
> >> > > >> From: sa5bxt
> >> > > >> To: PPLL-VFO@yahoogroups.com
> >> > > >> Sent: Sunday, February 26, 2012 9:31 AM
> >> > > >> Subject: [PPLL-VFO] Re: Lower bands
> >> > > >>
> >> > > >>
> >> > > >>
> >> > > >> Hi
> >> > > >> While serching in my component boxes, I find a little prescaler
circuit,MC12080. It divide by 10,20,40,80. It was used
> >> > > >> in
> >> > > >> another VFO circuit i found on the net (Before I find the SI project!) Is it
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> >> > > >> >
> >> > > >> > Mats,
> >> > > >> > What you need following the flip-flops depends on what you want to do with
the signal.
> >> > > >> > It is a square wave at that point.
> >> > > >> > Best Regards,
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> >> > > >> >
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> >> > > >> > From: "sa5bxt" <mats.su@>
> >> > > >> > To: <PPLL-VFO@yahoogroups.com>
> >> > > >> > Sent: Thursday, February 23, 2012 1:04 PM
> >> > > >> > Subject: [PPLL-VFO] Re: Lower bands
> >> > > >> >

> >> > > >> >
> >> > > >> > > Thanks! I guess it must be fast 74-circuits so´I must do some shopping. Do I need some buffer on the output?
> >> > > >> > >
> >> > > >> > > Mats
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> >> > > >> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >> > > >> > >>
> >> > > >> > >> Mats,
> >> > > >> > >>
> >> > > >> > >> Yes, you need to add some external circuitry to get the frequency down below 10 MHz.
> >> > > >> > >> Using two flip-flops to divide by 4 is the method used quite often, and the method I've used in some of my
> >> > > >> > >> sample designs in the FILES section. For a starter, see the mechanism in the front-end of my
> >> > > >> > >> Si570 CW Transmitter.
> >> > > >> > >>
> >> > > >> > >> By the way, you will notice that I have a couple of "Exclusive OR" gates in front of the two flip-flops.
> >> > > >> > >> You may be able to get along without them - feeding the Si570's 1.5v p-p signal right into the first
> >> > > >> > >> flip-flop and letting it trigger the second flip-flop. However, according to the flip-flop spec, 1.5v is not
> >> > > >> > >> quite enough for every part in every situation. Using the two "Exclusive OR" gates in front makes the
> >> > > >> > >> 1.5v signal "more robust" and then it will meet the spec requirements. Look back at message
> >> > > >> > >> number 184 and see more details of how the "Exclusive ORs" work in this circuit.
> >> > > >> > >>
> >> > > >> > >> Best Regards,
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> >> > > >> > >>
> >> > > >> > >>
> >> > > >> > >> ----- Original Message -----
> >> > > >> > >> From: "sa5bxt" <mats.su@>
> >> > > >> > >> To: <PPLL-VFO@yahoogroups.com>
> >> > > >> > >> Sent: Wednesday, February 22, 2012 5:23 AM
> >> > > >> > >> Subject: [PPLL-VFO] Lower bands
> >> > > >> > >>
> >> > > >> > >>
> >> > > >> > >> > Well, here I am again! My project run´s perfect. But, as a beginner in higher frequency, a new question pop´s up.
> >> > > >> how do
> >> > > >> I do
> >> > > >> > to

> >> > > >> > >> > get under 10Mhz? Divided by function get right frequncy on disply but not out. As you can see I´m using the
> >> > > >> "learning by
> >> > > >> doing"
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226. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-11 21:14:50 UTC
From: sa5bxt
Topic: 208 Message: 226

Hi again
Well while testing I probably blown up something. Just unstable 11MHz out. Hope it´s not the Si570. Time to sleep here now, see what tomorow brings!
Mats

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
>
> Hi Craig
> This is a real mystery! XOR works all the way up in frequency, flip flop´s just to 13-14MHz. I test with a new 74ac74, all th same!
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> Regards
> Mats
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> > You say "range is no problem and it follows perfectly when in divide by 1 mode". Does this mean that you can
> > look at the Si570 output (before it is divided) and you can count to higher frequencies? If so, it looks like the
> > XOR circuits or the flip flops are not keeping up. Strange.
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> > Anyone else have any ideas?
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> > ----- Original Message -----
> > From: "sa5bxt" <mats.su@>
> > To: <PPLL-VFO@yahoogroups.com>
> > Sent: Sunday, March 11, 2012 4:27 AM
> > Subject: [PPLL-VFO] Re: Lower bands
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> > > Hi!
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> > >> Did you include the "exclusive-or" circuitry in front of the flip-flops? This will make the driving signal from the SI570 a
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> > >> > > Getting the software to run with your new division factor is another issue. Of course changes could be made to the software
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> > >> > > From: "sa5bxt" <mats.su@>
> > >> > > To: <PPLL-VFO@yahoogroups.com>
> > >> > > Sent: Sunday, February 26, 2012 3:10 PM
> > >> > > Subject: [PPLL-VFO] Re: Lower bands
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> > >> > > >I agree, but I don´t think the frequency is the problem. It´s only dived by 10, so that probably leeds to new software, and
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227. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-12 17:48:44 UTC
From: sa5bxt
Topic: 208 Message: 227

Hi
Mayby something happend to microcontroller. LCD goes "on-off" suddenly there was text on row two. Rotating encoder slow brings up frequency to around 25MHz (correct reading on lcd) at that point frequency goes to 11-something MHz (lcd displays "correct" value only out frequency going low) even so while fast rotate encoder, LCD shows 10.000 MHZ while counter show 11xxxMHz). Tested 16F88 in my PIC kit2 reading device with no errors. Someone got any ideas?

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
>
> Hi again
> Well while testing I probably blown up something. Just unstable 11MHz out. Hope it´s not the Si570. Time to sleep here now, see what tomorow brings!
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> > > -Craig
> > >
> > > ----- Original Message -----
> > > From: "sa5bxt" <mats.su@>
> > > To: <PPLL-VFO@yahoogroups.com>
> > > Sent: Sunday, March 11, 2012 4:27 AM
> > > Subject: [PPLL-VFO] Re: Lower bands
> > >

> > >
> > > > Hi!
> > > >
> > > > I´m using first part of your 7MHz CW 74HC86 and 74AC74. Ouestion is if output is to low for my counter, it´s on the lowest
> > > > sensitivity (15mVrms). I (Think) noticed lower sensitivity at higher freqency. Range is no problem it follows perfect when in
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> > > >
> > > > Regards
> > > > Mats
> > > >
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> > > >>
> > > >> Mats,
> > > >>
> > > >> Don't know. As I recall, mine works up to at least 28 MHz .
> > > >>
> > > >> Did you include the "exclusive-or" circuitry in front of the flip-flops? This will make the driving signal from the SI570 a
> > > >> little more robust.
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> > > >> > > >> From: sa5bxt
> > > >> > > >> To: PPLL-VFO@yahoogroups.com
> > > >> > > >> Sent: Sunday, February 26, 2012 9:31 AM
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228. Re: [PPLL-VFO] Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-12 18:36:54 UTC
From: Justin Pinnix
Topic: 208 Message: 228

Check your voltage regulator. Mine stopped regulating and I was seeing weirdnesses in the display. After a few seconds, it would shut down as the bench supply went into current limiting. Then, I stupidly raised the current limit and smoked the LCD and PIC.

On Mon, Mar 12, 2012 at 1:48 PM, sa5bxt <mats.su@...> wrote:

> **
>
>
> Hi
> Mayby something happend to microcontroller. LCD goes "on-off" suddenly
> there was text on row two. Rotating encoder slow brings up frequency to
> around 25MHz (correct reading on lcd) at that point frequency goes to
> 11-something MHz (lcd displays "correct" value only out frequency going
> low) even so while fast rotate encoder, LCD shows 10.000 MHZ while counter
> show 11xxxMHz). Tested 16F88 in my PIC kit2 reading device with no errors.
> Someone got any ideas?
>
>
> --- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
> >
> > Hi again
> > Well while testing I probably blown up something. Just unstable 11MHz
> out. Hope it´s not the Si570. Time to sleep here now, see what tomorow
> brings!
> > Mats
> >
> > --- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@> wrote:
> > >
> > > Hi Craig
> > > This is a real mystery! XOR works all the way up in frequency, flip
> flop´s just to 13-14MHz. I test with a new 74ac74, all th same!
> > >
> > > Regards
> > > Mats
> > >
> > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@>
> wrote:
> > > >
> > > > Hi Mats,
> > > > I'm not sure what the problem is. You should have plenty of output
> from the flip-flops to measure in your counter.
> > > > You say "range is no problem and it follows perfectly when in divide
> by 1 mode". Does this mean that you can

> > > > look at the Si570 output (before it is divided) and you can count to
> higher frequencies? If so, it looks like the
> > > > XOR circuits or the flip flops are not keeping up. Strange.
> > > >
> > > > Anyone else have any ideas?
> > > >
> > > > -Craig
> > > >
> > > > ----- Original Message -----
> > > > From: "sa5bxt" <mats.su@>
> > > > To: <PPLL-VFO@yahoogroups.com>
> > > > Sent: Sunday, March 11, 2012 4:27 AM
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229. Re: Lower bands

Yahoo group: PPLL-VFO
Date: 2012-03-21 19:16:52 UTC
From: sa5bxt
Topic: 208 Message: 229

It was the microcontroller that "blow up". I probably did not clean my workspace, so some little bit of a component leg make a shortcircuit. So now it works perfect again. In desperation I orderd a new Si570! But then a bright idea come up! I´m order a set of bareboards from kanga and build a stand alone VFO/Signalgenerator for comming experiments.
73 de
Mats

--- In PPLL-VFO@yahoogroups.com, Justin Pinnix <justin.pinnix@...> wrote:
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> Check your voltage regulator. Mine stopped regulating and I was seeing
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> > > >
> > > --- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@> wrote:
> > > > >
> > > > Hi Craig
> > > > This is a real mystery! XOR works all the way up in frequency, flip
> > flop´s just to 13-14MHz. I test with a new 74ac74, all th same!
> > > > >
> > > > Regards
> > > > Mats

> > > >
> > > > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@>
> > wrote:
> > > > >
> > > > > Hi Mats,
> > > > > I'm not sure what the problem is. You should have plenty of output
> > from the flip-flops to measure in your counter.
> > > > > You say "range is no problem and it follows perfectly when in divide
> > by 1 mode". Does this mean that you can
> > > > > look at the Si570 output (before it is divided) and you can count to
> > higher frequencies? If so, it looks like the
> > > > > XOR circuits or the flip flops are not keeping up. Strange.
> > > > > >
> > > > > Anyone else have any ideas?
> > > > > >
> > > > > -Craig
> > > > > >
> > > > > ----- Original Message -----
> > > > > From: "sa5bxt" <mats.su@>
> > > > > To: <PPLL-VFO@yahoogroups.com>
> > > > > Sent: Sunday, March 11, 2012 4:27 AM
> > > > > Subject: [PPLL-VFO] Re: Lower bands
> > > > > >
> > > > > >
> > > > > > Hi!
> > > > > > >
> > > > > > I´m using first part of your 7MHz CW 74HC86 and 74AC74. Ouestion
> > is if output is to low for my counter, it´s on the lowest
> > > > > > sensitivity (15mVrms). I (Think) noticed lower sensitivity at
> > higher freqency. Range is no problem it follows perfect when in
> > > > > > divide by "1" mode. Do I need some kind of buffer amp after
> > flip-flop?
> > > > > > >
> > > > > > Regards
> > > > > > Mats
> > > > > > >
> > > > > > --- In PPLL-VFO@yahoogroups.com, "AA0ZZ" <aa0zz@> wrote:
> > > > > > >>
> > > > > > >> Mats,
> > > > > > >>
> > > > > > >> Don't know. As I recall, mine works up to at least 28 MHz .
> > > > > > >>
> > > > > > >> Did you include the "exclusive-or" circuitry in front of the
> > flip-flops? This will make the driving signal from the SI570 a
> > > > > > >> little more robust.
> > > > > > >>
> > > > > > >> Best Regards,
> > > > > > >> -Craig, AA0ZZ
> > > > > > >>
> > > > > > >>

> > > > > >> --- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@> wrote:
> > > > > >> >
> > > > > >> > My divide by 4 works nice, but it stops round 14MHz. Is this
> > due to 74 logic? I´m using HC and AC. Another question is if RF
> > > > > >> > output could go direct to VFO input at my SSB transciver?
> > > > > >> > Mats
> > > > > >> >
> > > > > >> > --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@>
> > wrote:
> > > > > >> > >
> > > > > >> > > Mats,
> > > > > >> > >
> > > > > >> > > Yes, it's always interesting to try things.
> > > > > >> > >
> > > > > >> > > Getting the software to run with your new division factor is
> > another issue. Of course changes could be made to the software
> > > > > >> > > to
> > > > > >> > > display the correct frequency, since "it's just code". The
> > source code is there but it would take a considerable amount
> > > > > >> > > of work. The current display routine just divides the
> > frequency by 2 or 4 (if the "divide-by-x" flag is set) by simply
> > > > > >> > > shifting the
> > > > > >> > > Si570 frequency by 1or 2. The new display routine would need
> > a much more complicated algorithm.
> > > > > >> > > Best Regards,
> > > > > >> > > -Craig, AA0ZZ
> > > > > >> > >
> > > > > >> > >
> > > > > >> > > ----- Original Message -----
> > > > > >> > > From: "sa5bxt" <mats.su@>
> > > > > >> > > To: <PPLL-VFO@yahoogroups.com>
> > > > > >> > > Sent: Sunday, February 26, 2012 3:10 PM
> > > > > >> > > Subject: [PPLL-VFO] Re: Lower bands
> > > > > >> > >
> > > > > >> > >
> > > > > >> > > >I agree, but I don´t think the frequency is the problem.
> > It´s only dived by 10, so that probably leeds to new software, and
> > > > > >> > > >much of
> > > > > >> > > >the quality of Si project is gone (I think!). So I work´s
> > on with my 74 logic that been proven work perfect. But some
> > > > > >> > > >brainstorming is never wrong for creativity!
> > > > > >> > > > 73 de
> > > > > >> > > > Mats
> > > > > >> > > >
> > > > > >> > > > --- In PPLL-VFO@yahoogroups.com, "Jim or Cathy Wallace"
> > <jimandcathywallace@> wrote:
> > > > > >> > > > >
> > > > > >> > > > >> Just from glancing at the data sheet, I suspect the answer
> > is no. This part is intended for operation at 1 gHz. The
> > > > > >> > > > >> graph of

> > > > > >> > > >> their operating "window" stops at 100 mHz, so you still
> > might not get the range you want. Input levels run around 100 mV
> > > > > > >> > > >> and
> > > > > > > >> > > >> output around 1 volt p-p, which might not be enough for
> > what you want. But, you've got the part, so what's the harm in
> > > > > > > >> > > >> trying it
> > > > > > > >> > > >> out? Experiment.
> > > > > > > >> > > >>
> > > > > > > >> > > >> Jim
> > > > > > > >> > > >> KB5MT
> > > > > > > >> > > >> ----- Original Message -----
> > > > > > > >> > > >> From: sa5bxt
> > > > > > > >> > > >> To: PPLL-VFO@yahoogroups.com
> > > > > > > >> > > >> Sent: Sunday, February 26, 2012 9:31 AM
> > > > > > > >> > > >> Subject: [PPLL-VFO] Re: Lower bands
> > > > > > > >> > > >>
> > > > > > > >> > > >>
> > > > > > > >> > > >>
> > > > > > > >> > > >> Hi
> > > > > > > >> > > >> While serching in my component boxes, I find a little
> > prescaler circuit,MC12080. It divide by 10,20,40,80. It was used
> > > > > > > >> > > >> in
> > > > > > > >> > > >> another VFO circuit i found on the net (Before I find the
> > SI project!) Is it possible to use that to get lower frequency?
> > > > > > > >> > > >> 73 de
> > > > > > > >> > > >> Mats
> > > > > > > >> > > >>
> > > > > > > >> > > >> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ"
> > <aa0zz@> wrote:
> > > > > > > >> > > >>
> > > > > > > >> > > >> Mats,
> > > > > > > >> > > >> What you need following the flip-flops depends on what
> > you want to do with the signal.
> > > > > > > >> > > >> It is a square wave at that point.
> > > > > > > >> > > >> Best Regards,
> > > > > > > >> > > >> -Craig, AA0ZZ
> > > > > > > >> > > >>
> > > > > > > >> > > >> ----- Original Message -----
> > > > > > > >> > > >> From: "sa5bxt" <mats.su@>
> > > > > > > >> > > >> To: <PPLL-VFO@yahoogroups.com>
> > > > > > > >> > > >> Sent: Thursday, February 23, 2012 1:04 PM
> > > > > > > >> > > >> Subject: [PPLL-VFO] Re: Lower bands
> > > > > > > >> > > >>
> > > > > > > >> > > >>
> > > > > > > >> > > >> Thanks! I guess it must be fast 74-circuits so´I must
> > do some shopping. Do I need some buffer on the output?
> > > > > > > >> > > >>
> > > > > > > >> > > >> Mats
> > > > > > > >> > > >>
> > > > > > > >> > > >> --- In PPLL-VFO@yahoogroups.com, "Craig Johnson,

> > AA0ZZ" <aa0zz@> wrote:
> > > > > >> > > >> > >>
> > > > > > >> > > >> > >> Mats,
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >> Yes, you need to add some external circuitry to get
> > the frequency down below 10 MHz.
> > > > > > >> > > >> > >> Using two flip-flops to divide by 4 is the method
> > used quite often, and the method I've used in some of my
> > > > > > >> > > >> > >> sample designs in the FILES section. For a starter,
> > see the mechanism in the front-end of my
> > > > > > >> > > >> > >> Si570 CW Transmitter.
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >> By the way, you will notice that I have a couple of
> > "Exclusive OR" gates in front of the two flip-flops.
> > > > > > >> > > >> > >> You may be able to get along without them - feeding
> > the Si570's 1.5v p-p signal right into the first
> > > > > > >> > > >> > >> flip-flop and letting it trigger the second
> > flip-flop. However, according to the flip-flop spec, 1.5v is not
> > > > > > >> > > >> > >> quite enough for every part in every situation. Using
> > the two "Exclusive OR" gates in front makes the
> > > > > > >> > > >> > >> 1.5v signal "more robust" and then it will meet the
> > spec requirements. Look back at message
> > > > > > >> > > >> > >> number 184 and see more details of how the "Exclusive
> > ORs" work in this circuit.
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >> Best Regards,
> > > > > > >> > > >> > >> -Craig, AA0ZZ
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >> ----- Original Message -----
> > > > > > >> > > >> > >> From: "sa5bxt" <mats.su@>
> > > > > > >> > > >> > >> To: <PPLL-VFO@yahoogroups.com>
> > > > > > >> > > >> > >> Sent: Wednesday, February 22, 2012 5:23 AM
> > > > > > >> > > >> > >> Subject: [PPLL-VFO] Lower bands
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >>
> > > > > > >> > > >> > >> > Well, here I am again! My project run´s perfect.
> > But, as a beginner in higher frequency, a new question pop´s up.
> > > > > > >> > > how do
> > > > > > >> > > I do
> > > > > > >> > > >> > > to
> > > > > > >> > > >> > > get under 10Mhz? Divided by function get right
> > frequncy on disply but not out. As you can see I´m using the
> > > > > > >> > > "learning by
> > > > > > >> > > doing"
> > > > > > >> > > >> > > and "trial and error" methods in my way to become
> > aham radio amateur.

> > > > > >> > > >> > >> > 73 de
> > > > > >> > > >> > >> > Mats
> > > > > >> > > >> > >> >
> > > > > >> > > >> > >> >
> > > > > >> > > >> > >> >
> > > > > >> > > >> > >> > ------------------------------------
> > > > > >> > > >> > >> >
> > > > > >> > > >> > >> > Yahoo! Groups Links
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> > > > > >> > > >> > >
> > > > > >> > > >> > > ------------------------------------
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> > > > > >> > > >> > > Yahoo! Groups Links
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> > > > > >> > > > Yahoo! Groups Links
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> > > > > > Yahoo! Groups Links
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230. I need help :-)

Yahoo group: PPLL-VFO
Date: 2012-05-30 01:05:45 UTC
From: py2gac
Topic: 230 Message: 230

hello
I need help!

I rode the circuit, just shows the splash screen does not change frequently.
the only output 10 MHZ.

thank

231. shows only the routine display_version! :-(

Yahoo group: PPLL-VFO
Date: 2012-06-08 15:38:56 UTC
From: py2gac
Topic: 231 Message: 231

Do not enter into calibration mode.

somebody help me?

232. Re: shows only the routine display_version! :-) - Resolved

Yahoo group: PPLL-VFO
Date: 2012-06-19 16:05:01 UTC
From: AA0ZZ
Topic: 231 Message: 232

This issue has been resolved offline. It was an I2C communications failure. Signals were not being passed between the PIC and the Si570. Reheating the solder connections resolved the issue and now all is well.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "py2gac" <py2gac@...> wrote:
>
> Do not enter into calibration mode.
>
> somebody help me?
>

233. si570 project

Yahoo group: PPLL-VFO
Date: 2012-07-21 04:23:29 UTC
From: kehamby
Topic: 233 Message: 233

hi. I'm just getting back to work on the project.
How do I obtain the pic16f88 with AA0ZZ software installed??Also I read an article somewhere about a pic emulator/developer software package; recommended as a must have.
Please help.
Thanks 73
Ken K4DRL

234. PIC for Si570 Project

Yahoo group: PPLL-VFO
Date: 2012-07-21 09:16:54 UTC
From: n8et@woh.rr.com
Topic: 234 Message: 234

There should have been one in the project kit (Control Board)I shipped to you. Let me know if there was not and I will get one on the way.

If you did not get the Control Board (using the PICEL III as the controller) you will need to download it from Craig's web page and load it yourself.

73 - Bill - N8ET

235. SI570 cmos output compatability

Yahoo group: PPLL-VFO
Date: 2012-08-09 14:37:01 UTC
From: pauldebono@rocketmail.com
Topic: 235 Message: 235

Can I drive the 74S74 flip flop directly from SI570cmos version,(as used on the daughter board) or do I need any buffers/convertors ? I did experiment some time ago, but cannot remember the outcome.

236. Re: SI570 cmos output compatability

Yahoo group: PPLL-VFO
Date: 2012-08-11 00:26:51 UTC
From: AA0ZZ
Topic: 235 Message: 236

Hi Paul,

Yes, you can drive 74xx74 flip-flops directly from the CMOS Si570. I have done it, and I know it does work. However, if you look carefully at the 74xx74 spec sheet you will see that the 1.5v square wave is not quite enough according to the "rules". It will work - most of the time - but it is not guaranteed to work with all parts in all situations. That's why the spec sheet says what it does.

Instead, I would suggest you try a trick" that was shown to me by my good friend, Don Huff, W6JL. He suggests front-ending the 74xx74 flip-flops with a pair of XOR gates. I have a write-up in the files section that explains this technique. It's in the folder: "AA0ZZ - usage schematics and diagrams". The file called "W6JL Trick using XOR gates to drive flip-flops" explains the trick. You can see the technique being used in my schematic called "CWXmtr-V2d Schematic". Try it!

What do you think? Comments welcome.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "pauldebono@..." <vpt7388@...> wrote:
>
> Can I drive the 74S74 flip flop directly from SI570cmos version,(as used on the daughter board) or do I need any buffers/convertors ? I did experiment some time ago, but cannot remember the outcome.
>

237. different versions

Yahoo group: PPLL-VFO
Date: 2012-08-11 05:40:25 UTC
From: pauldebono@rocketmail.com
Topic: 237 Message: 237

Whats the major difference between board version 1.3 and 1.6 ?
Do I have to do any modification to drive a version 1.3 daughter board with a controller board version 1.6 ??

238. Re: [PPLL-VFO] different versions

Yahoo group: PPLL-VFO
Date: 2012-08-11 15:55:15 UTC
From: Craig Johnson, AA0ZZ
Topic: 237 Message: 238

Hi Paul,

The latest version of the control board is now v1.9. The changes have all been slight, and the daughterboard connections have not
changed. In versioin 1.3 I was trying to prepare in advance for the possibility of using another type of Si570 in the daughtercard
so there were two outputs. The second output is not connected to the CMOS version of the Si570. I have since given up on that
idea for now, so the new v1.9 control board only has one path from the daughterboard connector to the board edge. The new one is made for a surface mount SMA edge connector so no need to solder coax to the board.
Also improved the ground plane a bit. However, these are all relatively small changes.

Bottom line - your v1.3 control board will work fine with the daughterboard. Just have to look at the output signal and make sure
it is clean and sufficient amplitude. My latest gives a nice 1.5v square wave when sent into a 50 ohm load.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "pauldebono@..." <pawlud@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Saturday, August 11, 2012 12:40 AM
Subject: [PPLL-VFO] different versions

> Whats the major difference between board version 1.3 and 1.6 ?
> Do I have to do any modification to drive a version 1.3 daughter board with a controller board version 1.6 ??
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
>
>
>

239. Sideband Select Pulse from the PIC's RA6 and RA7

Yahoo group: PPLL-VFO
Date: 2012-08-21 23:44:14 UTC
From: ab6wl
Topic: 239 Message: 239

Hello Craig,

My Si570 Daughtercard & Control Board seem to be working well together, except that I am not seeing any pulse from the PIC output ports RA6 or RA7 (pins pins 15 & 16) when I change from "U" to "L" or vice versa in the menu. The same is true when I connect the Daughtercard and PIC to my PIC-EL III. I am using a Tektronix 1012B in Single Seq mode with a trigger level of 1V to capture the pulse.

Earle

240. Re: Sideband Select Pulse from the PIC's RA6 and RA7

Yahoo group: PPLL-VFO
Date: 2012-08-27 23:10:23 UTC
From: AA0ZZ
Topic: 239 Message: 240

Hi Earl,

Sorry for the very late reply. I saw it and started thinking about it but it got away from me before I could investigate.

Today I did some checking, using a simulator and also my hardware.

It does work, but it may work differently than what you expected.
A 12 ms low pulse appears on pin RA7 (pin 16) when you LEAVE THE MENU win LSB or - mode.
A 12 ms low pulse appears on pin RA6 (pin 15) when you LEAVE THE MENU win USB or + mode.

This way the relay doesn't clatter as you mess around in the menu.

Hope this works for you. If not, let me know and I can change it to pulse on every change in the menu.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "ab6wl" <ecraig@...> wrote:
>
> Hello Craig,
>
> My Si570 Daughtercard & Control Board seem to be working well together, except that I am not seeing any pulse from the PIC output ports RA6 or RA7 (pins pins 15 & 16) when I change from "U" to "L" or vice versa in the menu. The same is true when I connect the Daughtercard and PIC to my PIC-EL III. I am using a Tektronix 1012B in Single Seq mode with a trigger level of 1V to capture the pulse.
>
> Earle
>

241. Re: [PPLL-VFO] Re: Sideband Select Pulse from the PIC's RA6 and RA7

Yahoo group: PPLL-VFO
Date: 2012-08-28 05:00:22 UTC
From: Earle Craig
Topic: 239 Message: 241

Hello Craig,

Thank you for providing the helpful information. Yes, my expectations were different, and I will adjust them accordingly. Your reasoning definitely makes sense--reducing the relay clatter to a minimum.

All the best,

Earle
AB6WL

On Aug 27, 2012, at 4:10 PM, AA0ZZ wrote:

Hi Earl,

Sorry for the very late reply. I saw it and started thinking about it but it got away from me before I could investigate.

Today I did some checking, using a simulator and also my hardware.

It does work, but it may work differently than what you expected.
A 12 ms low pulse appears on pin RA7 (pin 16) when you LEAVE THE MENU win LSB or - mode.
A 12 ms low pulse appears on pin RA6 (pin 15) when you LEAVE THE MENU win USB or + mode.

This way the relay doesn't clatter as you mess around in the menu.

Hope this works for you. If not, let me know and I can change it to pulse on every change in the menu.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "ab6wl" <ecraig@...> wrote:
>
> Hello Craig,
>
> My Si570 Daughtercard & Control Board seem to be working well together, except that I am not seeing any pulse from the PIC output ports RA6 or RA7 (pins pins 15 & 16) when I change from "U" to "L" or vice versa in the menu. The same is true when I connect the Daughtercard and PIC to my PIC-EL III. I am using a Tektronix 1012B in Single Seq mode with a trigger level of 1V to capture the pulse.
>
> Earle
>

242. No freq change V7.7A

Yahoo group: PPLL-VFO
Date: 2012-08-30 10:09:38 UTC
From: sjef44
Topic: 242 Message: 242

Hello Craig

Thanks to your excellent documentation, I was able to make the control and daughterboard myself.
I have a lvds Si570 10-260 MHz.
In the V7.7A asm file I changed the default freq by removing the ";" four times for the defaultsifreq 56,320 MHz and adding these in front of the 10 MHz.
The display is looking ok. Freq is changing, pushbutons working and the menu is working on the display.
But the freq of the SI570 is always 56,320 MHz on my freq. counter.
On the oscilloscoop, I can see the freq. changing when I rotate the encoder, but the freq is always going back to 56.320 MHz.
I tried the daugtherboard seperately on a breadbord with a picaxe chip and a simple program. That works.
I tried the control and daughterboard with a simple picbasic program, that is working too.
Finally I found on arrl.org/qexfiles version V7.6A. I changed the defaultfrequentie and assembled with MPLAB IDE V8.84, like I did before with version 7.7A. I programmed the Pic16F88 with my homemade Pickit2.
Now everything is working, on the second line I get the registers.
Looks like it is always in debug mode?

Excellent design and documentation.
Thanks Craig sharing your design with us.

Regard Sjef PA0SJK

243. Output waveform

Yahoo group: PPLL-VFO
Date: 2012-09-03 08:51:17 UTC
From: sa5bxt
Topic: 243 Message: 243

Hi!

Just back to my radio project (short visit in audio electronics...). Starting with my Si 570 Vfo. It´s working nice when change frequency. But I have some questions about output. I´s not squarewave,, what I see on my Velleman PC100 pc scope is a sinusoidal and output 1,4V to 1,6V.
Question is if I´d, in some unknown way, blow up the Si circuit? I build it from a kit from kanga.

Is it also possible that this can explain my problems with the divid by four circuit? As we talked about in another tread.

73de
SA5BXT
Mats Sundström

244. Re: [PPLL-VFO] Output waveform

Yahoo group: PPLL-VFO
Date: 2012-09-03 15:20:51 UTC
From: Craig Johnson, AA0ZZ
Topic: 243 Message: 244

Hi Mats,

Your Si570 is probably working just fine. I don't know what frequency you are measuring but it is possible that your oscilloscope
is not telling you the "full truth". Have you looked at the voltage directly out of the Si570 pins before going to any external
circuitry? It may be that you are losing some of the signal farther down in the chain. The 1.6 v p-p signal that I show in the
QEX article is with coax from the control board RF jack directly to a 50-ohm input to the oscilloscope. If you don't have a 50
ohm load, the reading could be misleading.

Are you using the control board from Kanga? Or are you using your own?

I looked back in the archives for the other thread and your difficulties with the divide by four circuitry. Yes, if you are not
getting "enough" signal, you could have trouble in switching the following flip-flops. Did you see the file called "W6JL trick
using XOR gates to drive flip-flops" ? If you aren't using this, it may help you. If you are, in fact, only getting 200 mv p-p out
of your Si570. It could be a bad Si570 but I have never seen that problem. They either work or they don't work.

I would say you should go ahead and try it with the XOR gate front end and see if it's enough signal to trigger your following
circuits.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "sa5bxt" <mats.su@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Monday, September 03, 2012 3:51 AM
Subject: [PPLL-VFO] Output waveform

> Hi!
>
> Just back to my radio project (short visit in audio electronics...). Starting with my Si 570 Vfo. It?s working nice when change
> frequency. But I have some questions about output. I?s not squarewave,, what I see on my Velleman PC100 pc scope is a sinusoidal
> and output 1,4V to 1,6V.
> Question is if I?d, in some unknown way, blow up the Si circuit? I build it from a kit from kanga.
>
> Is it also possible that this can explain my problems with the divid by four circuit? As

we talked about in another tread.
>
> 73de
> SA5BXT
> Mats Sundstr?m
>
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> Yahoo! Groups Links
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>

245. Re: Output waveform

Yahoo group: PPLL-VFO
Date: 2012-09-04 19:41:33 UTC
From: sa5bxt
Topic: 243 Message: 245

Hi!

Fast answer as usual! Thanks! There is a differens, I have 1,6volts on Si output, lose 0,4volts after R6. I have a short RG174 cable from Rf out to panel jack. There is no differens if I take away this cable, measure 0,4volts less after R6 (Rf out jack). Possible to short R6?

Divide circuit from W6JL works nice up to 10Mhz (40 Mhz out from Si), then flip-flops don´t work. Lost to many mV´s moving upwards in frequency?

As I can se my VFO works perfekt, my counter and VFO show´s the same frequency, so hope Si circuit is ok.

My scope go up to 12Mhz so it´s probably not true what I measure. I´m going to get a 50ohm terminal plug.

I´m using kanga motherboard.

Regards

Mats Sundström
SA5BXT

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mats,
>
> Your Si570 is probably working just fine. I don't know what frequency you are measuring but it is possible that your oscilloscope
> is not telling you the "full truth". Have you looked at the voltage directly out of the Si570 pins before going to any external
> circuitry? It may be that you are losing some of the signal farther down in the chain. The 1.6 v p-p signal that I show in the
> QEX article is with coax from the control board RF jack directly to a 50-ohm input to the oscilloscope. If you don't have a 50
> ohm load, the reading could be misleading.
>
> Are you using the control board from Kanga? Or are you using your own?
>
> I looked back in the archives for the other thread and your difficulties with the divide by four circuitry. Yes, if you are not
> getting "enough" signal, you could have trouble in switching the following flip-flops. Did you see the file called "W6JL trick
> using XOR gates to drive flip-flops" ? If you aren't using this, it may help you. If you are, in fact, only getting 200 mv p-p out
> of your Si570. It could be a bad Si570 but I have never seen that problem. They either work or they don't work.

>
> I would say you should go ahead and try it with the XOR gate front end and see if it's enough signal to trigger your following
> circuits.
>
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Monday, September 03, 2012 3:51 AM
> Subject: [PPLL-VFO] Output waveform
>
>
> > Hi!
> >
> > Just back to my radio project (short visit in audio electronics...). Starting with my Si 570 Vfo. It´s working nice when change
> > frequency. But I have some questions about output. I´s not squarewave,, what I see on my Velleman PC100 pc scope is a sinusoidal
> > and output 1,4V to 1,6V.
> > Question is if I´d, in some unknown way, blow up the Si circuit? I build it from a kit from kanga.
> >
> > Is it also possible that this can explain my problems with the divid by four circuit? As we talked about in another tread.
> >
> > 73de
> > SA5BXT
> > Mats Sundström
> >
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> > ------------------------------------
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> > Yahoo! Groups Links
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246. RE: [PPLL-VFO] Re: Output waveform

Yahoo group: PPLL-VFO
Date: 2012-09-04 20:26:31 UTC
From: pbunn
Topic: 243 Message: 246
Attachments: 3 described; binary payloads are missing from this source WARC

A 12 MHz scope can't even dream about displaying a square wave of more than 4 Mhz and it won't do much of a job on that. A square wave is composed the fundamental and all odd order harmonics. If you can't even see the 3rd harmonics - it looks like somewhat like a sine wave. If it is a digital scope - it is likely a poor performer at the max rating (12 MHz). You scope is acting as a filter allowing only the fundamental to be observed.

N4LTA

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com] On Behalf Of sa5bxt
Sent: Tuesday, September 04, 2012 3:42 PM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Re: Output waveform

Hi!

Fast answer as usual! Thanks! There is a differens, I have 1,6volts on Si output, lose 0,4volts after R6. I have a short RG174 cable from Rf out to panel jack. There is no differens if I take away this cable, measure 0,4volts less after R6 (Rf out jack). Possible to short R6?

Divide circuit from W6JL works nice up to 10Mhz (40 Mhz out from Si), then flip-flops don´t work. Lost to many mV´s moving upwards in frequency?

As I can se my VFO works perfekt, my counter and VFO show´s the same frequency, so hope Si circuit is ok.

My scope go up to 12Mhz so it´s probably not true what I measure. I´m going to get a 50ohm terminal plug.

I´m using kanga motherboard.

Regards

Mats Sundström
SA5BXT

--- In PPLL-VFO@yahoogroups.com<mailto:PPLL-VFO%40yahoogroups.com>, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Hi Mats,
>
> Your Si570 is probably working just fine. I don't know what frequency you are measuring but it is possible that your oscilloscope
> is not telling you the "full truth". Have you looked at the voltage directly out of the Si570 pins before going to any external
> circuitry? It may be that you are losing some of the signal farther down in the chain. The 1.6 v p-p signal that I show in the

> QEX article is with coax from the control board RF jack directly to a 50-ohm input to the oscilloscope. If you don't have a 50
> ohm load, the reading could be misleading.
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> Are you using the control board from Kanga? Or are you using your own?
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> I looked back in the archives for the other thread and your difficulties with the divide by four circuitry. Yes, if you are not
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> of your Si570. It could be a bad Si570 but I have never seen that problem. They either work or they don't work.
>
> I would say you should go ahead and try it with the XOR gate front end and see if it's enough signal to trigger your following
> circuits.
>
> Best Regards,
> -Craig, AA0ZZ
>
> ----- Original Message -----
> From: "sa5bxt" <mats.su@...>
> To: <PPLL-VFO@yahoogroups.com<mailto:PPLL-VFO%40yahoogroups.com>>
> Sent: Monday, September 03, 2012 3:51 AM
> Subject: [PPLL-VFO] Output waveform
>
>
> > Hi!
> >
> > Just back to my radio project (short visit in audio electronics...). Starting with my Si 570 Vfo. It´s working nice when change
> > frequency. But I have some questions about output. I´s not squarewave,, what I see on my Velleman PC100 pc scope is a sinusoidal
> > and output 1,4V to 1,6V.
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> > 73de
> > SA5BXT
> > Mats Sundström
> >
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> > ------------------------------------
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> > Yahoo! Groups Links
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247. Re: Output waveform

Yahoo group: PPLL-VFO
Date: 2012-09-05 09:00:59 UTC
From: sa5bxt
Topic: 243 Message: 247

Hi

Thanks for the information. This was as I thougt. My PC-scope was first intended to be used in audo and control applicatins, a work it does well. A "real" scope is high on my wish list! Had to trust on my frequency counter. Seem´s I had to suppose that wave form is ok. Most likely it is, I hope?

Regards

sa5bxt
Mats Sundström

--- In PPLL-VFO@yahoogroups.com, pbunn <pbunn@...> wrote:
>
> A 12 MHz scope can't even dream about displaying a square wave of more than 4 Mhz and it won't do much of a job on that. A square wave is composed the fundamental and all odd order harmonics. If you can't even see the 3rd harmonics - it looks like somewhat like a sine wave. If it is a digital scope - it is likely a poor performer at the max rating (12 MHz). You scope is acting as a filter allowing only the fundamental to be observed.
> N4LTA
>
>
> From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com] On Behalf Of sa5bxt
> Sent: Tuesday, September 04, 2012 3:42 PM
> To: PPLL-VFO@yahoogroups.com
> Subject: [PPLL-VFO] Re: Output waveform
>
>
>
> Hi!
>
> Fast answer as usual! Thanks! There is a differens, I have 1,6volts on Si output, lose 0,4volts after R6. I have a short RG174 cable from Rf out to panel jack. There is no differens if I take away this cable, measure 0,4volts less after R6 (Rf out jack). Possible to short R6?
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> My scope go up to 12Mhz so it´s probably not true what I measure. I´m going to get a 50ohm terminal plug.
>

> I´m using kanga motherboard.
>
> Regards
>
> Mats Sundström
> SA5BXT
>
> --- In PPLL-VFO@yahoogroups.com<mailto:PPLL-VFO%40yahoogroups.com>, "Craig Johnson, AA0ZZ" <aa0zz@> wrote:
> >
> > Hi Mats,
> >
> > Your Si570 is probably working just fine. I don't know what frequency you are measuring but it is possible that your oscilloscope
> > is not telling you the "full truth". Have you looked at the voltage directly out of the Si570 pins before going to any external
> > circuitry? It may be that you are losing some of the signal farther down in the chain. The 1.6 v p-p signal that I show in the
> > QEX article is with coax from the control board RF jack directly to a 50-ohm input to the oscilloscope. If you don't have a 50
> > ohm load, the reading could be misleading.
> >
> > Are you using the control board from Kanga? Or are you using your own?
> >
> > I looked back in the archives for the other thread and your difficulties with the divide by four circuitry. Yes, if you are not
> > getting "enough" signal, you could have trouble in switching the following flip-flops. Did you see the file called "W6JL trick
> > using XOR gates to drive flip-flops" ? If you aren't using this, it may help you. If you are, in fact, only getting 200 mv p-p out
> > of your Si570. It could be a bad Si570 but I have never seen that problem. They either work or they don't work.
> >
> > I would say you should go ahead and try it with the XOR gate front end and see if it's enough signal to trigger your following
> > circuits.
> >
> > Best Regards,
> > -Craig, AA0ZZ
> >
> > ----- Original Message -----
> > From: "sa5bxt" <mats.su@>
> > To: <PPLL-VFO@yahoogroups.com<mailto:PPLL-VFO%40yahoogroups.com>>
> > Sent: Monday, September 03, 2012 3:51 AM
> > Subject: [PPLL-VFO] Output waveform
> >
> >
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> > > 73de
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> > > Mats Sundström
> > >
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> > > Yahoo! Groups Links
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248. Default Frequency and LCD Readout

Yahoo group: PPLL-VFO
Date: 2012-10-14 22:54:23 UTC
From: ab6wl
Topic: 248 Message: 248

Hello Craig,

I was reading through your conversation with Mats, SA5BXT, and I have the same question. I suspect that Mats had gone into the Menu and set the "Frequency Division for LCD Display" to 4, because, in this mode, my display reads 7.200.000 at start-up. Nevertheless, the actual measured default start-up frequency is the expected 10MHz.

When I set the "Frequency Division for LCD Display" to 2, the display reads 14.400.000 at start-up and likewise 28.800.000 when set to 1 at start-up. Yet, as I said, the actual measured frequency is 10MHz.

Any thoughts?

Earle
AB6WL

249. Re: [PPLL-VFO] Default Frequency and LCD Readout

Yahoo group: PPLL-VFO
Date: 2012-10-15 01:42:54 UTC
From: Craig Johnson, AA0ZZ
Topic: 248 Message: 249

Earle,
What version of the software are you running?
Are you using the daughtercard and / or control board?
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ab6wl" <ecraig@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, October 14, 2012 5:54 PM
Subject: [PPLL-VFO] Default Frequency and LCD Readout

> Hello Craig,
>
> I was reading through your conversation with Mats, SA5BXT, and I have the same question. I suspect that Mats had gone into the
> Menu and set the "Frequency Division for LCD Display" to 4, because, in this mode, my display reads 7.200.000 at start-up.
> Nevertheless, the actual measured default start-up frequency is the expected 10MHz.
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> When I set the "Frequency Division for LCD Display" to 2, the display reads 14.400.000 at start-up and likewise 28.800.000 when
> set to 1 at start-up. Yet, as I said, the actual measured frequency is 10MHz.
>
> Any thoughts?
>
> Earle
> AB6WL
>
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> Yahoo! Groups Links
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250. Re: [PPLL-VFO] Default Frequency and LCD Readout

Yahoo group: PPLL-VFO
Date: 2012-10-15 04:39:48 UTC
From: Earle Craig
Topic: 248 Message: 250

Hello Craig,

I just figured out what is going on. I had completely forgotten about the feature of pressing and holding Pushbutton 3 for longer than 2 seconds to store the current frequency in EEPROM (page 6 in the Daughtercard manual). I must have done this for 7.200MHz. However, the actual measured frequency at start-up is still 10MHz, and I am running version 7.7 of PEgen570 using both the Daughtercard and Control Board. I even just changed the stored frequency to 14.200MHz, and the start-up frequency is still 10MHz. Then, when I adjust the frequency up .001kHz, the output changes to 56.800MHz (since I have set the "Frequency Division for LCD Display" to 4).

So, is this what I should expect?

Thanks,

Earle
AB6WL

On Oct 14, 2012, at 6:42 PM, Craig Johnson, AA0ZZ wrote:

Earle,
What version of the software are you running?
Are you using the daughtercard and / or control board?
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "ab6wl" <ecraig@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Sunday, October 14, 2012 5:54 PM
Subject: [PPLL-VFO] Default Frequency and LCD Readout

> Hello Craig,
>
> I was reading through your conversation with Mats, SA5BXT, and I have the same question. I suspect that Mats had gone into the
> Menu and set the "Frequency Division for LCD Display" to 4, because, in this mode, my display reads 7.200.000 at start-up.
> Nevertheless, the actual measured default start-up frequency is the expected 10MHz.
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> When I set the "Frequency Division for LCD Display" to 2, the display reads 14.400.000 at start-up and likewise 28.800.000 when
> set to 1 at start-up. Yet, as I said, the actual measured frequency is 10MHz.
>
> Any thoughts?
>
> Earle

> AB6WL
>
>
>
> ------------------------------------
>
> Yahoo! Groups Links
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>

251. Input level

Yahoo group: PPLL-VFO
Date: 2012-11-29 20:14:31 UTC
From: sa5bxt
Topic: 251 Message: 251

Hi
Whats tje normal level on the signal level in to trx? Is it possible to connect My Si vfo direct to trx?
regards
SA5BXT Mats

252. Re: Input level

Yahoo group: PPLL-VFO
Date: 2012-11-30 02:45:01 UTC
From: AA0ZZ
Topic: 251 Message: 252

Hi Mats,

--- In PPLL-VFO@yahoogroups.com, "sa5bxt" <mats.su@...> wrote:
>
> Hi
> Whats tje normal level on the signal level in to trx? Is it possible to connect My Si vfo direct to trx?
> regards
> SA5BXT Mats
>
The Si570 puts out about 1.5v p-p into 50 ohms. How much drive you need depends on your transmitter.

If you are going to be using a divide-by-4 mechanism for generating quadrature signals, you may be interested in the discussion we had a while back. Look back at messages around 235 and 236 for information about driving flip-flops.

Best Regards,
-Craig, AA0ZZ

253. ponderings on DDS VFO use

Yahoo group: PPLL-VFO
Date: 2013-01-19 01:46:16 UTC
From: brianpepperdine
Topic: 253 Message: 253

Hi. Just joined up. I have a general set of query here..hopefully not too outlandish or sky-high. In part its been in my mind for few years now re. old gear..tubes and such, but also in relation to Drake stuff.
You'll see. I had this ready to go to the QRP mail list, but thought I would post it here since I recently started to go back to the Web stuff I'd read on DDS VFOs and the info Bill Kelsey has on Craig's project and the original related articles.
Please let me know IF and WHERE I am crazy or misleading myself.

I got a NorCal FCC1/FCC2 VFO some time back and now am thinking about how I can employ it and/or related devices that are available.
One thing I think I'd LIKE to do with it is to be the VFO for my Rick Campbell R1 receiver (though I do have an air-cap based
Universal VFO for 40m for it). Or the MicroR2.

But..thinking about that.. the main reason I'd like to use it is that the FCC VFO and other DDS VFO devices tune a lot lot slower than
our conventional bare-bones QRP rigs that use single-turn pots or variable air caps. For me, I like it to be SLOW going across the band (which is why I miss availability of 3-turn pots... though 10-turn ones work they are very slow to get up and down.. the opposite problem!).

Air caps suffer similarly unless you get a good 6:1 vernier on there, IMHO.

What I'd like to know is.. has anyone found it useful to go in to the VFO-in point on things like the SWL rigs, NorCal 40 or Sierra, Emtech, etc and put in a external VFO line to a DDS VFO? Simple substitute for the local oscillator set appropriately to the mixing scheme?

I originally got the DDS VFO idea hoping to substitute it for old fashioned (unobtainium) tube VFOs such as the Heath HG-10, Hallicrafters or Johson V-122 via buffer/amp and avoid the trouble of hard-to-get drifty/chirpy tube VFOs or of course in the same vein replace the crystals used in older rigs or even Drake rigs (get WARC bands, get shortwave bands).

Anyhow, thinking out loud via the List, since there are pretty good DDS VFOs out there aside from the NorCal FCC.

Or does this fly in the face of the simplicity and portability of the small qrp rigs? Though one could build the DDS in the rig with no issue I suspect, if one did not one to tie into an external DDS 'umbilical' of a DDS being employed in multiple situations.

The small simple rigs are fun, but the bands are crowded and busy.. its nice to be able to fine tune into the signals. Hear them and work them.

Similarly, I feel that some old classic stuff is missing out on being easily used due to the difficulty of old/tube VFOs or crystal availability.

Brien
VE3VAW

254. Alternative to the PEgen570

Yahoo group: PPLL-VFO
Date: 2013-03-07 03:59:59 UTC
From: serracin7388
Topic: 254 Message: 254

Looking for alternative software for the pic, to drive the SI570

255. And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-08 06:53:40 UTC
From: Joel
Topic: 255 Message: 255

In the process of moving my signal generator into a new box, I wired up the power backwards. This is a combo stand alone controller/daughter board. It smoked out the 5 volt regulator on the controller board and popped the electrolytic. But other than that I can't find anything wrong. Well, except now it don't work. The 570 puts out a constant 10Mhz no matter how I spin the encoder. I scoped the leads from the encoder and I see they are both pulsing when I spin it. The display shows just the normal PEgen570 display without any frequency. So I burned a new 16f88 with the 7.7 code but it acts the same. The 2 i2c lines are at 3 volts p2p with data at the 570. So I think that looks okay too. So I'm stumped. Wouldn't the display show the frequency even if there was no 570? Or is there some sort of feedback needed? I don't have a spare 570, but certainly would replace it if it looks like its bad. But considering it's sending out the default frequency and the display don't show any frequency, it seems like the problem is elsewhere? Any trouble shooting words of wisdom for a klutz like me?

Joe AG4QC

256. Re: [PPLL-VFO] And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-09 22:12:31 UTC
From: Craig Johnson, AA0ZZ
Topic: 255 Message: 256

Joe,
It sounds like your PIC is still not talking to the Si570.
I will send you a new version of the code by private Email to try.
The frequency could still be changing and the code still not sending good info to the Si570.
Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: "Joel" <ag4qc@...>
To: <PPLL-VFO@yahoogroups.com>
Sent: Friday, March 08, 2013 12:53 AM
Subject: [PPLL-VFO] And it went --Poof --

> In the process of moving my signal generator into a new box, I wired up the power backwards. This is a combo stand alone
> controller/daughter board. It smoked out the 5 volt regulator on the controller board and popped the electrolytic. But other than
> that I can't find anything wrong. Well, except now it don't work. The 570 puts out a constant 10Mhz no matter how I spin the
> encoder. I scoped the leads from the encoder and I see they are both pulsing when I spin it. The display shows just the normal
> PEgen570 display without any frequency. So I burned a new 16f88 with the 7.7 code but it acts the same. The 2 i2c lines are at 3
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> there was no 570? Or is there some sort of feedback needed? I don't have a spare 570, but certainly would replace it if it looks
> like its bad. But considering it's sending out the default frequency and the display don't show any frequency, it seems like the
> problem is elsewhere? Any trouble shooting words of wisdom for a klutz like me?
>
> Joe AG4QC
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> Yahoo! Groups Links
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257. Re: And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-09 22:38:05 UTC
From: Stephen Farthing
Topic: 255 Message: 257

Joel,

When you say the 570 puts out a constant 10 MHz is this because you heard it on an Rx or just saw it on the display? I am no expert with PICs but are you sure the fuses are set correctly?

73s Steve

258. Re: [PPLL-VFO] Re: And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-10 00:55:20 UTC
From: Craig Johnson, AA0ZZ
Topic: 255 Message: 258

Steve,
The version of Si570 that I use in the kits has a default start-up frequency of 10 MHz so that's what appears when no parameters are sent to it.
Best Regards,
-Craig
----- Original Message -----
From: Stephen Farthing
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, March 09, 2013 4:38 PM
Subject: [PPLL-VFO] Re: And it went --Poof --

Joel,

When you say the 570 puts out a constant 10 MHz is this because you heard it on an Rx or just saw it on the display? I am no expert with PICs but are you sure the fuses are set correctly?

73s Steve

259. Re: And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-10 18:04:58 UTC
From: Joel
Topic: 255 Message: 259

I burned a new 16f88 with the new code and it's more or less the same issue. I do now show version 7.9b but no actual frequency on the display. The 570 is receiving 3 volts of data on pins 7 and 8. I am looking at it with a scope, so can't really decipher the data's contents. I also replaced the two level converters on those lines just in case that was an issue. So I guess I'm left with the 570. I have sent a couple emails to Kanga to order another board/kit and am awaiting their reply. I figure to just replace the whole board as for the price of the complete kit isn't much more then the cost of the 570.

I sort of figured the PIC would send the data to the 570 and then display the corresponding frequency on the display. Yeah, the 570 puts out the 10Mhz by default, as I remember when I first built it I just applied power the the board, without the control board and it came up with a nice 10Hmz signal.

Anyway, I suppose the 570's data input leads must be the issue. As I'm sure they are sensitive to my power issue. I just love this as I use it a lot as a signal generator. Just too bad I wasn't more careful plugging in the power connector on the control board. I see a diode across the line and a fuse in it's future.

Thanks,
Joe AG4QC

--- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote:
>
> Joe,
> It sounds like your PIC is still not talking to the Si570.
> I will send you a new version of the code by private Email to try.
> The frequency could still be changing and the code still not sending good info to the Si570.
> Best Regards,
> -Craig, AA0ZZ
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> From: "Joel" <ag4qc@...>
> To: <PPLL-VFO@yahoogroups.com>
> Sent: Friday, March 08, 2013 12:53 AM
> Subject: [PPLL-VFO] And it went --Poof --
>
>
> > In the process of moving my signal generator into a new box, I wired up the power backwards. This is a combo stand alone
> > controller/daughter board. It smoked out the 5 volt regulator on the controller board and popped the electrolytic. But other than
> > that I can't find anything wrong. Well, except now it don't work. The 570 puts out a constant 10Mhz no matter how I spin the
> > encoder. I scoped the leads from the encoder and I see they are both pulsing when I

spin it. The display shows just the normal
> > PEgen570 display without any frequency. So I burned a new 16f88 with the 7.7 code but it acts the same. The 2 i2c lines are at 3
> > volts p2p with data at the 570. So I think that looks okay too. So I'm stumped. Wouldn't the display show the frequency even if
> > there was no 570? Or is there some sort of feedback needed? I don't have a spare 570, but certainly would replace it if it looks
> > like its bad. But considering it's sending out the default frequency and the display don't show any frequency, it seems like the
> > problem is elsewhere? Any trouble shooting words of wisdom for a klutz like me?
> >
> > Joe AG4QC
> >
> >
> >
> >
> > ------------------------------------
> >
> > Yahoo! Groups Links
> >
> >
> >
>

260. Re: [PPLL-VFO] Re: And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-10 20:07:36 UTC
From: Stephen Farthing
Topic: 255 Message: 260

Hi Craig,

I understand that. I have a few of them in various projects and find them pretty robust to ill treatment. I am not an expert at Pics but I assume that you programmed it with the correct fuse settings for the type of clock you are using.

73s Steve

On 10 March 2013 00:55, Craig Johnson, AA0ZZ <aa0zz@...> wrote:

> **
>
>
> **
> Steve,
> The version of Si570 that I use in the kits has a default start-up
> frequency of 10 MHz so that's what appears when no parameters are sent to
> it.
> Best Regards,
> -Craig
>
> ----- Original Message -----
> *From:* Stephen Farthing <squirrox@...>
> *To:* PPLL-VFO@yahoogroups.com
> *Sent:* Saturday, March 09, 2013 4:38 PM
> *Subject:* [PPLL-VFO] Re: And it went --Poof --
>
> Joel,
>
> When you say the 570 puts out a constant 10 MHz is this because you heard
> it on an Rx or just saw it on the display? I am no expert with PICs but
> are you sure the fuses are set correctly?
>
> 73s Steve
>
>
>

261. Re: [PPLL-VFO] Re: And it went --Poof --

Yahoo group: PPLL-VFO
Date: 2013-03-10 21:00:13 UTC
From: Will
Topic: 255 Message: 261

Joe,

Sorry to be deliverer of bad news but Bill Kelsey of Kanga was taken to hospital about a week ago after a stroke. That means that Kanga wil be shut down for some time. No emails or other queries will be answered in the mean time.

We all send our support to him and his wife

Cheers
Will
ZL1TAO

----- Original Message -----
From: Joel
Sent: 03/11/13 07:04 AM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Re: And it went --Poof --

I burned a new 16f88 with the new code and it's more or less the same issue. I do now show version 7.9b but no actual frequency on the display. The 570 is receiving 3 volts of data on pins 7 and 8. I am looking at it with a scope, so can't really decipher the data's contents. I also replaced the two level converters on those lines just in case that was an issue. So I guess I'm left with the 570. I have sent a couple emails to Kanga to order another board/kit and am awaiting their reply. I figure to just replace the whole board as for the price of the complete kit isn't much more then the cost of the 570. I sort of figured the PIC would send the data to the 570 and then display the corresponding frequency on the display. Yeah, the 570 puts out the 10Mhz by default, as I remember when I first built it I just applied power the the board, without the control board and it came up with a nice 10Hmz signal. Anyway, I suppose the 570's data input leads must be the issue. As I'm sure they are sensitive to my power issue. I just love this as I use it a lot as a signal generator. Just too bad I wasn't more careful plugging in the power connector on the control board. I see a diode across the line and a fuse in it's future. Thanks, Joe AG4QC --- In PPLL-VFO@yahoogroups.com, "Craig Johnson, AA0ZZ" <aa0zz@...> wrote: > > Joe, > It sounds like your PIC is still not talking to the Si570. > I will send you a new version of the code by private Email to try. > The frequency could still be changing and the code still not sending good info to the Si570. > Best Regards, > -Craig, AA0ZZ > > > ----- Original Message ----- > From: "Joel" <ag4qc@...> > To: <PPLL-VFO@yahoogroups.com> > Sent: Friday, March 08, 2013 12:53 AM > Subject: [PPLL-VFO] And it went --Poof -- > > > > In the process of moving my signal generator into a new box, I wired up the power backwards. This is a combo stand alone > > controller/daughter board. It smoked out the 5 volt regulator on the controller board and popped the electrolytic. But other than > > that I can't find anything wrong. Well, except now it don't work. The 570 puts out a constant 10Mhz no matter how I spin the > > encoder. I scoped the leads from the encoder and I see they are both pulsing when I spin it. The display shows just the normal > > PEgen570 display without any frequency. So I burned a new 16f88 with the 7.7 code but it acts the same. The 2 i2c lines are at 3 > > volts p2p with data at the 570. So I think that looks okay too. So I'm

stumped. Wouldn't the display show the frequency even if > > there was no 570? Or is there some sort of feedback needed? I don't have a spare 570, but certainly would replace it if it looks > > like its bad. But considering it's sending out the default frequency and the display don't show any frequency, it seems like the > > problem is elsewhere? Any trouble shooting words of wisdom for a klutz like me? > > > > Joe AG4QC > > > > > > > > > > > > ---------- > > > > Yahoo! Groups Links > > > > > > >

262. The SI570 controller

Yahoo group: PPLL-VFO
Date: 2013-04-06 19:41:05 UTC
From: serracin7388
Topic: 262 Message: 262

Just finished the controller, programmed for division by four and I have this issue:

Startup frequency 7Mhz

When moving the cursor to change frequency, the frequency goes up to 25Mhz, sometimes 27Mhz (that's the maximum) and the pic freezes- I cannot go up nor down.

Have to re-set, by switching off and on the 12 volts supply. There must be a reset point somewhere, without having to switch the supply.

When I go down the frequency, as soon as I pass 2Mhz, the display shows 31Mhz, sometimes 32Mhz, and it freezes, no up nor down.

Paul

263. More on the SI570 controller

Yahoo group: PPLL-VFO
Date: 2013-04-07 11:33:32 UTC
From: serracin7388
Topic: 262 Message: 263

I have two controller chips. The second one was programmed by the latest version from AA0ZZ. It work s ok, but the SI570 remains static on 10.00Mhz

Paul

--- In PPLL-VFO@yahoogroups.com, "serracin7388" <serracin7388@...> wrote:
>
> Just finished the controller, programmed for division by four and I have this issue:
>
> Startup frequency 7Mhz
>
> When moving the cursor to change frequency, the frequency goes up to 25Mhz, sometimes 27Mhz (that's the maximum) and the pic freezes- I cannot go up nor down.
>
> Have to re-set, by switching off and on the 12 volts supply. There must be a reset point somewhere, without having to switch the supply.
>
> When I go down the frequency, as soon as I pass 2Mhz, the display shows 31Mhz, sometimes 32Mhz, and it freezes, no up nor down.
>
> Paul
>

264. Any PCB boards or parts kits available?

Yahoo group: PPLL-VFO
Date: 2013-04-28 17:14:26 UTC
From: mwmansfield
Topic: 264 Message: 264

Hello everyone!

I just joined the group here and would really like to build a receiver for the "space fence" at 216.9 MHz.

From everything I've read about this setup, it should work great as I just need a good USB receiver for this frequency that is accurate on frequency and has good sensitivity.

Any help or pointers to parts kits or PCB availability would be greatly appreciated.

Thanks in advance!
73,
Mark

265. Any PCB boards or parts kits available?

Yahoo group: PPLL-VFO
Date: 2013-04-28 17:57:24 UTC
From: mwmansfield
Topic: 264 Message: 265

Hello everyone!

I just joined the group here and would really like to build a receiver for the "space fence" at 216.9 MHz.

From everything I've read about this setup, it should work great as I just need a good USB receiver for this frequency that is accurate on frequency and has good sensitivity.

Any help or pointers to parts kits or PCB availability would be greatly appreciated.

Thanks in advance!
73,
Mark

266. Any PCB boards or parts kits available?

Yahoo group: PPLL-VFO
Date: 2013-04-28 17:57:38 UTC
From: mwmansfield
Topic: 264 Message: 266

Hello everyone!

I just joined the group here and would really like to build a receiver for the "space fence" at 216.9 MHz.

From everything I've read about this setup, it should work great as I just need a good USB receiver for this frequency that is accurate on frequency and has good sensitivity.

Any help or pointers to parts kits or PCB availability would be greatly appreciated.

Thanks in advance!
73,
Mark

267. Re: Any PCB boards or parts kits available?

Yahoo group: PPLL-VFO
Date: 2013-04-29 19:28:19 UTC
From: serracin7388@...
Topic: 264 Message: 267

have you ever considered a dongle ? see here:

http://sivantoledotech.wordpress.com/2012/04/25/dvbt-dongle/

268. Re: ponderings on DDS VFO use

Yahoo group: PPLL-VFO
Date: 2013-04-29 23:58:22 UTC
From: kb5zxm
Topic: 253 Message: 268

I am looking at doing the same, but in hopes of bring back old test equipment, and making it more freq agile. Or adding these circuits to existing things still in use like a freq counter to my buddy's Heath Kit modulation monitor, and making use of old commercial radios , that are still good and tough ,just need batteries.have to figure how to handle multi ctcss aspect.
I have been getting old tv test equip for the boxes, to make stuff in, like ntsc gen, or sig level meters, will save a lot of work, and may have room for a battery.
SO >>You see I am one of 'those' that should not be allowed free run at a swap meet with out ADULT Supervision.
so far the freq meter is all I have added. as far as the other I am trying to learn to progr. in C++ with the help of kd2kw, also on this list, but temp out of pocket.
Darrell kb5zxm@... , Magnolia tex.

--- In PPLL-VFO@yahoogroups.com, "brianpepperdine" <brianpepperdine@...> wrote:
>
> Hi. Just joined up. I have a general set of query here..hopefully not too outlandish or sky-high. In part its been in my mind for few years now re. old gear..tubes and such, but also in relation to Drake stuff.
> You'll see. I had this ready to go to the QRP mail list, but thought I would post it here since I recently started to go back to the Web stuff I'd read on DDS VFOs and the info Bill Kelsey has on Craig's project and the original related articles.
> Please let me know IF and WHERE I am crazy or misleading myself.
>
>
> I got a NorCal FCC1/FCC2 VFO some time back and now am thinking about how I can employ it and/or related devices that are available.
> One thing I think I'd LIKE to do with it is to be the VFO for my Rick Campbell R1 receiver (though I do have an air-cap based
> Universal VFO for 40m for it). Or the MicroR2.
>
> But..thinking about that.. the main reason I'd like to use it is that the FCC VFO and other DDS VFO devices tune a lot lot slower than
> our conventional bare-bones QRP rigs that use single-turn pots or variable air caps. For me, I like it to be SLOW going across the band (which is why I miss availability of 3-turn pots... though 10-turn ones work they are very slow to get up and down.. the opposite problem!).
>
> Air caps suffer similarly unless you get a good 6:1 vernier on there, IMHO.
>
> What I'd like to know is.. has anyone found it useful to go in to the VFO-in point on things like the SWL rigs, NorCal 40 or Sierra, Emtech, etc and put in a external VFO line to a DDS VFO? Simple substitute for the local oscillator set appropriately to the mixing scheme?
>
> I originally got the DDS VFO idea hoping to substitute it for old fashioned (unobtainium)

tube VFOs such as the Heath HG-10, Hallicrafters or Johson V-122 via buffer/amp and avoid the trouble of hard-to-get drifty/chirpy tube VFOs or of course in the same vein replace the crystals used in older rigs or even Drake rigs (get WARC bands, get shortwave bands).
>
> Anyhow, thinking out loud via the List, since there are pretty good DDS VFOs out there aside from the NorCal FCC.
>
> Or does this fly in the face of the simplicity and portability of the small qrp rigs? Though one could build the DDS in the rig with no issue I suspect, if one did not one to tie into an external DDS 'umbilical' of a DDS being employed in multiple situations.
>
> The small simple rigs are fun, but the bands are crowded and busy.. its nice to be able to fine tune into the signals. Hear them and work them.
>
> Similarly, I feel that some old classic stuff is missing out on being easily used due to the difficulty of old/tube VFOs or crystal availability.
>
> Brien
> VE3VAW
>

269. Re: Any PCB boards or parts kits available?

Yahoo group: PPLL-VFO
Date: 2013-04-30 00:01:26 UTC
From: kb5zxm
Topic: 264 Message: 269

There is an article in QST magazine recently about this or similar doings

--- In PPLL-VFO@yahoogroups.com, serracin7388@... wrote:
>
> have you ever considered a dongle ? see here:
>
> http://sivantoledotech.wordpress.com/2012/04/25/dvbt-dongle/
>

270. Re: ponderings on DDS VFO use

Yahoo group: PPLL-VFO
Date: 2013-04-30 12:07:09 UTC
From: serracin7388@...
Topic: 253 Message: 270

The R2PRO and similar receivers/transceivers that use the same local oscillator , as the operating frequency suffer from hum. And it is very difficult to control, unless you have a perfect ground system in the shack.
A much better way nowadays are the QSD based transceivers, see here : http://yu1lm.qrpradio.com/, and because the local oscillator is running at times 4 the operating frequency, no hum is heard. Also a switch mixer is very sensitive and extremely low noise , compared to the traditional diode bridge !

271. Got the WA6UFQ Si570 card working with the AA0ZZ PIC program

Yahoo group: PPLL-VFO
Date: 2013-05-14 01:35:55 UTC
From: wa5bdu
Topic: 271 Message: 271

Hi Craig & fellow Si570 users. I bought the little Si570 card a few years ago but didn't get the controller card. As far as I'd gotten was to do a little bit of demo type stuff with the Arduino.

So recently I put a 16F88 with programming header on a Radio Shack proto board and added the stuff needed to make Craig's program talk to my Si570. It came up at around 14.012 MHz while showing 14.025, but after I did the calibrate routine it came right in like magic to within the accuracy of my counter. Using the slightly different Si570 card didn't really cause much of a problem, but having the level shifters off of the Si570 board did have me scratching my head for a minute.

I worked W6JL on CW some time back and he gave me such a compelling sales pitch for the all hardware phasing type receiver I decided I'd eventually have to give it a try. I'm poring over the R2 based circuit in QEX, the NC2030, W6JL's stuff and more, trying to decide which way I want to go. Should be fun.

Now I have to finish up this conventional receiver I've had at the 90% complete mark for several years, then move on to the Si570 / Tayloe detector thing.

73-

Nick, WA5BDU

272. Re: Got the WA6UFQ Si570 card working with the AA0ZZ PIC program

Yahoo group: PPLL-VFO
Date: 2013-05-14 16:36:11 UTC
From: aa0zz
Topic: 271 Message: 272

Hi Nick,
Great! Glad you got it working. Not bad for a little, tiny PIC, huh?

Will be looking to see what kind of design you come up with for the phasing receiver. I'm anxious to see it.

Best Regards,
-Craig, AA0ZZ

--- In PPLL-VFO@yahoogroups.com, "wa5bdu" <kennnick@...> wrote:
>
> Hi Craig & fellow Si570 users. I bought the little Si570 card a few years ago but didn't get the controller card. As far as I'd gotten was to do a little bit of demo type stuff with the Arduino.
>
> So recently I put a 16F88 with programming header on a Radio Shack proto board and added the stuff needed to make Craig's program talk to my Si570. It came up at around 14.012 MHz while showing 14.025, but after I did the calibrate routine it came right in like magic to within the accuracy of my counter. Using the slightly different Si570 card didn't really cause much of a problem, but having the level shifters off of the Si570 board did have me scratching my head for a minute.
>
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>
> Now I have to finish up this conventional receiver I've had at the 90% complete mark for several years, then move on to the Si570 / Tayloe detector thing.
>
> 73-
>
> Nick, WA5BDU
>

273. controlling a Softrock with the AA0ZZ controller

Yahoo group: PPLL-VFO
Date: 2013-06-14 10:03:37 UTC
From: serracin7388
Topic: 273 Message: 273

I have built the Softrock Ensemble RXTX, originally an HF SDR transceiver

http://www.wb5rvz.org/ensemble_rxtx/index?projectId=14

I do not like pc controlled radios. I prefer standalone, which in my opinion, has a much lower noise than SDRs. In any case, I do not like too much bells and whistles. I use my own operating skills !

so, I have disconnected the Ensemble AVR controller section by connecting the AA0ZZ SI570 & controller to the T1, a BN43-2402 2 turn bifilar xformer, feeding directly to the 74S74. No need of any drivers etc. The rest to be done is to use an analogue all pass audio phase shift network for both tx and rx, and a mic amplifier. I intend to use the G3TDZ phasing unit, which is based on the old 2Q4 B&W two phase audio phase shift network.

Paul
9H1FQ

274. Re: [PPLL-VFO] controlling a Softrock with the AA0ZZ controller

Yahoo group: PPLL-VFO
Date: 2013-06-14 18:25:00 UTC
From: Zack Widup
Topic: 273 Message: 274

Interesting. I've thought of at least trying something about that.

Do you not use a computer at all? One of the real powers of the SDR receiver, and the main reason I bought Softrock Ensemble II kits for both HF and VHF, was the ability to see a 96 kHz section of spectrum on the bandscope on the computer.

73, Zack W9SZ

On Fri, Jun 14, 2013 at 5:03 AM, serracin7388 <serracin7388@...>wrote:

> I have built the Softrock Ensemble RXTX, originally an HF SDR transceiver
>
> http://www.wb5rvz.org/ensemble_rxtx/index?projectId=14
>
> I do not like pc controlled radios. I prefer standalone, which in my
> opinion, has a much lower noise than SDRs. In any case, I do not like too
> much bells and whistles. I use my own operating skills !
>
> so, I have disconnected the Ensemble AVR controller section by connecting
> the AA0ZZ SI570 & controller to the T1, a BN43-2402 2 turn bifilar xformer,
> feeding directly to the 74S74. No need of any drivers etc. The rest to be
> done is to use an analogue all pass audio phase shift network for both tx
> and rx, and a mic amplifier. I intend to use the G3TDZ phasing unit, which
> is based on the old 2Q4 B&W two phase audio phase shift network.
>
> Paul
> 9H1FQ
>
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>
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> Yahoo! Groups Links
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275. Re: [PPLL-VFO] controlling a Softrock with the AA0ZZ controller

Yahoo group: PPLL-VFO
Date: 2013-06-17 20:07:11 UTC
From: serracin7388@...
Topic: 273 Message: 275

Hi,
 no, with all due respect, I do not need any bells and whistles. I prefer to use my radio operator skills, no fancy filters, displays etc etc.
And, try to hear to a good analogue tayloe based phasing rig, and compare it to an SDR pc controlled. You should hear a big difference in the noise level !! The only issue, is when using a standalone SI570, controlled by iether an AVR or PIC, tends to produce some noise, during tuning, but can be reduced by the correct software , proper grounding techniques and careful screening.

Paul
9H1FQ

276. V7.7A software

Yahoo group: PPLL-VFO
Date: 2013-09-01 03:38:14 UTC
From: <garywinblad@...>
Topic: 276 Message: 276

Hello!
First post on this group, hopefully its still surviving the Yahoo destruction!
I am WB6OGD from El Dorado Hills, CA.
I've been a big fan of the Si570 chip since it was discovered by the Softrock40 group years ago.
My current project is a G3XJP Pic-A-Star transciever. I hope to bring it up using a Si570 for the master oscillator.. What I have been slowly working on for the last year or so is taking Craig's excellent PIC .asm code and porting it to a larger 18F PIC that will
hopefully become the single controller for my Pic-A-Star.
I am using my old proven code for the LCD, I2C, etc.

Is there any code beyond V7.7A???

I am seeing a problem in the CalcRFREQ routine. Try as I might, I just can not get it to give me the right answer. The only real problem I have been able to identify is that variable "temp1" is not getting initialized anywhere that I have found.

Any insight would be appreciated,
73,
Gary
WB6OGD

277. Re: [PPLL-VFO] V7.7A software

Yahoo group: PPLL-VFO
Date: 2013-09-01 13:21:21 UTC
From: Craig Johnson, AA0ZZ
Topic: 276 Message: 277

Hi Gary,

Yes, YAHOO has DESTROYED the groups, all in the name of making it different. It was not broken, as far as I was knew, and it certainly stinks now. Some day I may be able to post the cover picture again but I can't right now. Maybe someone has more information about this.

As for your problems with the PPLL code, I will talk to you offline about it. I am confident we can make the 16F88 version work.

Yes, I am working on a newer version with an 18F PIC but that's a ways out yet.

We will all be looking forward to hearing about your project as you proceed.

Best Regards,
-Craig, AA0ZZ

----- Original Message -----
From: garywinblad@...
To: PPLL-VFO@yahoogroups.com
Sent: Saturday, August 31, 2013 10:38 PM
Subject: [PPLL-VFO] V7.7A software

Hello!
First post on this group, hopefully its still surviving the Yahoo destruction!
I am WB6OGD from El Dorado Hills, CA.
I've been a big fan of the Si570 chip since it was discovered by the Softrock40 group years ago.
My current project is a G3XJP Pic-A-Star transciever. I hope to bring it up using a Si570 for the master oscillator.. What I have been slowly working on for the last year or so is taking Craig's excellent PIC .asm code and porting it to a larger 18F PIC that will
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I am using my old proven code for the LCD, I2C, etc.

Is there any code beyond V7.7A???

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Any insight would be appreciated,
73,
Gary
WB6OGD

278. RE: V7.7A software

Yahoo group: PPLL-VFO
Date: 2013-09-01 13:29:49 UTC
From: <aa0zz@...>
Topic: 276 Message: 278

"was knew" - now that's an interesting phrase. Sorry about that - have to proof read more closely before I hit send.

-Craig

--- In ppll-vfo@yahoogroups.com, <aa0zz@cbjohn.com> wrote:

☐
Hi Gary,

Yes, YAHOO has DESTROYED the groups, all in the name of making it different. It was not broken, as far as I was knew, and it certainly stinks now. Some day I may be able to post the cover picture again but I can't right now. Maybe someone has more information about this.

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Yes, I am working on a newer version with an 18F PIC but that's a ways out yet.

We will all be looking forward to hearing about your project as you proceed.

Best Regards,

-Craig, AA0ZZ

----- Original Message -----

From: garywinblad@comcast.net

To: PPLL-VFO@yahoogroups.com

Sent: Saturday, August 31, 2013 10:38 PM

Subject: [PPLL-VFO] V7.7A software

Hello!
First post on this group, hopefully its still surviving the Yahoo destruction!
I am WB6OGD from El Dorado Hills, CA.
I've been a big fan of the Si570 chip since it was discovered by the Softrock40 group years ago.
My current project is a G3XJP Pic-A-Star transciever. I hope to bring it up using a Si570 for the master oscillator.. What I have been slowly working on for the last year or so is taking Craig's excellent PIC .asm code and porting it to a larger 18F PIC that will
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Any insight would be appreciated,
73,
Gary
WB6OGD

279. Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-10-29 17:25:37 UTC
From: <mats.su@...>
Topic: 279 Message: 279

Hi!
Something happend to my VFO. Suddenly it show about 40KHz wrong according to my counter. I change daughterboard and PIC controller but fault is still there. Still left to change is encoder and display, There is a high noise in my trx while turning the encoder. There is no steps while turning encoder can´t remember if it was so. (It´s A while since I used this trx). I had problem with grounding maybe something happend.
73 de
Mats sa5bxt

280. RE: Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-11-09 02:34:39 UTC
From: <aa0zz@...>
Topic: 279 Message: 280

Hi Mats,
Yes, that's very strange.
Is the VFO wrong right from power-up, or does it go bad after you turn the encoder?
Best Regards,
-Craig, AA0ZZ

---In PPLL-VFO@yahoogroups.com, <mats.su@telia.com> wrote:

Hi!
Something happend to my VFO. Suddenly it show about 40KHz wrong according to my counter. I change daughterboard and PIC controller but fault is still there. Still left to change is encoder and display, There is a high noise in my trx while turning the encoder. There is no steps while turning encoder can´t remember if it was so. (It´s A while since I used this trx). I had problem with grounding maybe something happend.
73 de
Mats sa5bxt

281. RE: RE: Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-11-18 17:35:35 UTC
From: <mats.su@...>
Topic: 279 Message: 281

Hi!
It´s ok from start. Problem starts when turning encoder
Regards
Mats

---In PPLL-VFO@yahoogroups.com, <aa0zz@...> wrote:

Hi Mats,
Yes, that's very strange.
Is the VFO wrong right from power-up, or does it go bad after you turn the encoder?
Best Regards,
-Craig, AA0ZZ

---In PPLL-VFO@yahoogroups.com, <mats.su@...> wrote:

Hi!
Something happend to my VFO. Suddenly it show about 40KHz wrong according to my counter. I change daughterboard and PIC controller but fault is still there. Still left to change is encoder and display, There is a high noise in my trx while turning the encoder. There is no steps while turning encoder can´t remember if it was so. (It´s A while since I used this trx). I had problem with grounding maybe something happend.
73 de
Mats sa5bxt

282. RE: RE: RE: Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-11-22 03:58:47 UTC
From: <aa0zz@...>
Topic: 279 Message: 282

Mats,
The only thing I can suggest is to try another encoder.
Best Regards,
-Craig, AA0ZZ

---In PPLL-VFO@yahoogroups.com, <mats.su@telia.com> wrote:

Hi!
It´s ok from start. Problem starts when turning encoder
Regards
Mats

---In PPLL-VFO@yahoogroups.com, <aa0zz@...> wrote:

Hi Mats,
Yes, that's very strange.
Is the VFO wrong right from power-up, or does it go bad after you turn the encoder?
Best Regards,
-Craig, AA0ZZ

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73 de
Mats sa5bxt

283. RE: RE: RE: RE: Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-12-01 11:24:21 UTC
From: <mats.su@...>
Topic: 279 Message: 283

Hi
Yes I agree it must be the encoder. Just wonder if it is a 24 pulse encoder with "steps"?
Regards
sa5bxt Mats

---In PPLL-VFO@yahoogroups.com, <aa0zz@...> wrote:

Mats,
The only thing I can suggest is to try another encoder.
Best Regards,
-Craig, AA0ZZ

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It´s ok from start. Problem starts when turning encoder
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-Craig, AA0ZZ

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73 de
Mats sa5bxt

284. Re: [PPLL-VFO] RE: RE: RE: RE: Fault finding!

Yahoo group: PPLL-VFO
Date: 2013-12-02 02:38:59 UTC
From: Craig Johnson, AA0ZZ
Topic: 279 Message: 284

Mats,
Yes, the one I ship with the kits has 24 pulses per revolution and there are two pulses 90 degrees apart (quadrature) so there are 96 "transitions" per revolution. Just make sure your encoder has two signals with this 90-degree relationship and it will work fine.
Best Regards,
-Craig, AA0ZZ
----- Original Message -----
From: mats.su@...
To: PPLL-VFO@yahoogroups.com
Sent: Sunday, December 01, 2013 5:24 AM
Subject: [PPLL-VFO] RE: RE: RE: RE: Fault finding!

Hi

Yes I agree it must be the encoder. Just wonder if it is a 24 pulse encoder with "steps"?

Regards

sa5bxt Mats

---In PPLL-VFO@yahoogroups.com, <aa0zz@...> wrote:

Mats,

The only thing I can suggest is to try another encoder.

Best Regards,

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Hi!

It´s ok from start. Problem starts when turning encoder

Regards

Mats

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Hi Mats,

Yes, that's very strange.

Is the VFO wrong right from power-up, or does it go bad after you turn the encoder?

Best Regards,

-Craig, AA0ZZ

---In PPLL-VFO@yahoogroups.com, <mats.su@...> wrote:

Hi!

Something happend to my VFO. Suddenly it show about 40KHz wrong according to my counter. I change daughterboard and PIC controller but fault is still there. Still left to change is encoder and display, There is a high noise in my trx while turning the encoder. There is no steps while turning encoder can´t remember if it was so. (It´s A while since I used this trx). I had problem with grounding maybe something happend.

73 de

Mats sa5bxt

285. Suppressing noises from controllers

Yahoo group: PPLL-VFO
Date: 2014-01-06 16:17:10 UTC
From: <pawlud@...>
Topic: 285 Message: 285

Is there any home-brew and/ or commercial way to suppress noise from LCD screens and their ribbon cable? Screening the LCD screen is not enough.

Also, a way to filter the SCL and Data lines from the SI570, PIC and other controllers. I have seen some using bypass capacitors, but the choice of value is very very critical.

286. Error reading from EE-prom...

Yahoo group: PPLL-VFO
Date: 2014-09-06 07:37:54 UTC
From: sm0ohc@...
Topic: 286 Message: 286

Hello !

Trying to control a SR63ng:s si570.

First tried the 7.7a version and with that all in the display was ok but
the fq out was always 56.320.

Then loaded the 7.6 from qex-files and it works until you restart with s3
pushed to fetch the calibrating data from the si570 after that it is locked to
56.32 again (still all looks well in the display)

It seem it has to do with the eeprom-routines

any ideas ?

73:s de Kenneth / SM0OHC

287. RE: [PPLL-VFO] Error reading from EE-prom...

Yahoo group: PPLL-VFO
Date: 2014-09-06 13:27:06 UTC
From: Craig Johnson, AA0ZZ
Topic: 286 Message: 287

Hi Kenneth,

The symptoms you are describing makes it sound like you are using an Si570 with a default frequency of 56.320 MHz. They are quite common parts and used in many applications. When the calculated parameters are out of range for a part (or if the I2C communications fail) it always goes back to generating the default frequency. I use a Si570 with a default frequency of 10 MHz instead, meaning there are different parameters in the tables used for the parameter calculations. The part number specifies the default frequency and I use part number 570CBC000107DG. I suspect the “107” is something different in your Si570.

The code for the 56.320 MHz default part is in the source code but “commented off”. It is possible to locate this code, enable it, disable the 10 MHz table, re-assemble the code, and load it into your PIC. That should get you going.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Saturday, September 06, 2014 2:38 AM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Error reading from EE-prom...

Hello !

Trying to control a SR63ng:s si570.

First tried the 7.7a version and with that all in the display was ok but
the fq out was always 56.320.

Then loaded the 7.6 from qex-files and it works until you restart with s3
pushed to fetch the calibrating data from the si570 after that it is locked to
56.32 again (still all looks well in the display)

It seem it has to do with the eeprom-routines

any ideas ?

73:s de Kenneth / SM0OHC

288. RE: [PPLL-VFO] Error reading from EE-prom...

Yahoo group: PPLL-VFO
Date: 2014-09-07 07:34:58 UTC
From: sm0ohc@...
Topic: 286 Message: 288

Hello Craig !
Thank you for reply !

You were absolutly right, in the SR63ng there is a 570CAC000141G.

I found the lines in the asm and made the commenting/uncommenting
and re-assembled.
It works in the 7.6-version but with hex on the second line (debug) always there.
and a 10khz (x4-mode) fq-shift in U/L and +, but correct in - mode...

It still didn´t work in the 7.7 vesion though.

73:s de Kenneth / SM0OHC

289. Re: Error reading from EE-prom...

Yahoo group: PPLL-VFO
Date: 2014-09-07 07:55:40 UTC
From: sm0ohc@...
Topic: 286 Message: 289

Correction !!

Forget the comment about 10khz shift !

it works in +/- but when U and L i choosen it locked to 56.32 again
and doesn´t respond to to the encoder (good with debug after all HI).

73:s / K.

290. RE: [PPLL-VFO] Re: Error reading from EE-prom...

Yahoo group: PPLL-VFO
Date: 2014-09-07 12:31:30 UTC
From: Craig Johnson, AA0ZZ
Topic: 286 Message: 290

Kenneth,

Glad you got it working. Congratulations. Hope it works well for you.

Tell us more about your project when you get a chance.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Sunday, September 07, 2014 2:56 AM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Re: Error reading from EE-prom...

Correction !!

Forget the comment about 10khz shift !

it works in +/- but when U and L i choosen it locked to 56.32 again
and doesn´t respond to to the encoder (good with debug after all HI).

73:s / K.

291. Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-19 13:57:04 UTC
From: L.M. (Larry) Hicks
Topic: 291 Message: 291

Hi Craig...

I broke the switch part of the rotary encoder that came with your Si570 PLL kit that I got from Kanga. I can't find a part number or manufacturer for it. I used one that I had hanging around but it does not work well. Can I get the details on the rotary encoder that you used??

Many Thanks,
Larry. VO1HL

Sent from my ASUS Pad

292. Re: Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-19 21:39:43 UTC
From: aa0zz@...
Topic: 291 Message: 292

Larry, To be clear, there isn't a switch in these encoders. Just a plain encoder. One of the four pins is unused.
Best Regards,
-Craig, AA0ZZ

293. RE: [PPLL-VFO] Re: Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-19 21:47:59 UTC
From: Craig Johnson, AA0ZZ
Topic: 291 Message: 293

Larry,

Sorry, looks like my first message to you didn’t make it so here is a repeat.

There isn’t a part number for you or anyone else to order. I got them direct from China by buying a huge quantity. I agree that they are the nicest mechanical encoders that I have ever seen and they work well in this application. They don’t work quite as well as an optical encoder but they are MUCH less expensive too.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Friday, September 19, 2014 4:40 PM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] Re: Si570 rotary encoder

Larry,

To be clear, there isn't a switch in these encoders. Just a plain encoder. One of the four pins is unused.

Best Regards,

-Craig, AA0ZZ

294. Re: Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-19 21:49:28 UTC
From: aa0zz@...
Topic: 291 Message: 294

Hi Larry,

There isn't a part number for these encoders that you can use for ordering. I got them by buying a large quantity from China. I agree that they are quite unique in performance compared to normal mechanical encoders.

Please send me your name and address and I will send you one. Might have to charge you something for postage.

Best Regards,
-Craig, AA0ZZ

295. Re: [PPLL-VFO] Re: Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-21 17:24:30 UTC
From: L.M. (Larry) Hicks
Topic: 291 Message: 295

Hi Craig...

Thanks for the reply.

I sourced a rotary encoder (from work!!) and after a little experimentation, it works! The tuning action is a bit different because the new encoder has detents as you turn it. But I kinda like that! And it means there is no wiggle between digits. This one moves definitely from one rotary position to another.

Thank you for your kind offer. But I'm good now.

BTW. The Si570 project board that I got from Kanga is happily working in my little SDR camping transceiver. It runs about ten watts out class E with an efficiency between 82% to 89% depending on the part of 40 meters I am using.

I have had loads of fun with it. But it is too large for serious long haul biking and camping so I am building another one based on FFT with a crystal in the middle of the band and a high speed codec. This one'll be tiny. CW and SSB maybe on 20 meters this time. I hope to have it ready in the spring for biking adventures next year.

73,
Larry. VO1HL

Sent from my ASUS Pad

"aa0zz@cbjohn.com [PPLL-VFO]" <PPLL-VFO@yahoogroups.com> wrote:

>
>
>Hi Larry,
>
>
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>
>
>Please send me your name and address and I will send you one. Might have to charge you something for postage.
>
>
>Best Regards,
>
>-Craig, AA0ZZ
>
>
>

>
>
><!-- #ygrp-mkp { border: 1px solid #d8d8d8; font-family: Arial; margin: 10px 0; padding: 0 10px; } #ygrp-mkp hr { border: 1px solid #d8d8d8; } #ygrp-mkp #hd { color: #628c2a; font-size: 85%; font-weight: 700; line-height: 122%; margin: 10px 0; } #ygrp-mkp #ads { margin-bottom: 10px; } #ygrp-mkp .ad { padding: 0 0; } #ygrp-mkp .ad p { margin: 0; } #ygrp-mkp .ad a { color: #0000ff; text-decoration: none; } #ygrp-sponsor #ygrp-lc { font-family: Arial; } #ygrp-sponsor #ygrp-lc #hd { margin: 10px 0px; font-weight: 700; font-size: 78%; line-height: 122%; } #ygrp-sponsor #ygrp-lc .ad { margin-bottom: 10px; padding: 0 0; } #actions { font-family: Verdana; font-size: 11px; padding: 10px 0; } #activity { background-color: #e0ecee; float: left; font-family: Verdana; font-size: 10px; padding: 10px; } #activity span { font-weight: 700; } #activity span:first-child { text-transform: uppercase; } #activity span a { color: #5085b6; text-decoration: none; } #activity span span { color: #ff7900; } #activity span .underline { text-decoration: underline; } .attach { clear: both; display: table; font-family: Arial; font-size: 12px; padding: 10px 0; width: 400px; } .attach div a { text-decoration: none; } .attach img { border: none; padding-right: 5px; } .attach label { display: block; margin-bottom: 5px; } .attach label a { text-decoration: none; } blockquote { margin: 0 0 0 4px; } .bold { font-family: Arial; font-size: 13px; font-weight: 700; } .bold a { text-decoration: none; } dd.last p a { font-family: Verdana; font-weight: 700; } dd.last p span { margin-right: 10px; font-family: Verdana; font-weight: 700; } dd.last p span.yshortcuts { margin-right: 0; } div.attach-table div div a { text-decoration: none; } div.attach-table { width: 400px; } div.file-title a, div.file-title a:active, div.file-title a:hover, div.file-title a:visited { text-decoration: none; } div.photo-title a, div.photo-title a:active, div.photo-title a:hover, div.photo-title a:visited { text-decoration: none; } div#ygrp-mlmsg #ygrp-msg p a span.yshortcuts { font-family: Verdana; font-size: 10px; font-weight: normal; } .green { color: #628c2a; } .MsoNormal { margin: 0 0 0 0; } o { font-size: 0; } #photos div { float: left; width: 72px; } #photos div div { border: 1px solid #666666; height: 62px; overflow: hidden; width: 62px; } #photos div label { color: #666666; font-size: 10px; overflow: hidden; text-align: center; white-space: nowrap; width: 64px; } #reco-category { font-size: 77%; } #reco-desc { font-size: 77%; } .replbq { margin: 4px; } #ygrp-actbar div a:first-child { /* border-right: 0px solid #000;*/ margin-right: 2px; padding-right: 5px; } #ygrp-mlmsg { font-size: 13px; font-family: Arial, helvetica,clean, sans-serif; *font-size: small; *font: x-small; } #ygrp-mlmsg table { font-size: inherit; font: 100%; } #ygrp-mlmsg select, input, textarea { font: 99% Arial, Helvetica, clean, sans-serif; } #ygrp-mlmsg pre, code { font:115% monospace; *font-size:100%; } #ygrp-mlmsg * { line-height: 1.22em; } #ygrp-mlmsg #logo { padding-bottom: 10px; } #ygrp-msg p a { font-family: Verdana; } #ygrp-msg p#attach-count span { color: #1E66AE; font-weight: 700; } #ygrp-reco #reco-head { color: #ff7900; font-weight: 700; } #ygrp-reco { margin-bottom: 20px; padding: 0px; } #ygrp-sponsor #ov li a { font-size: 130%; text-decoration: none; } #ygrp-sponsor #ov li { font-size: 77%; list-style-type: square; padding: 6px 0; } #ygrp-sponsor #ov ul { margin: 0; padding: 0 0 0 8px; } #ygrp-text { font-family: Georgia; } #ygrp-text p { margin: 0 0 1em 0; } #ygrp-text tt { font-size: 120%; } #ygrp-vital ul li:last-child { border-right: none !important; } -->

296. RE: [PPLL-VFO] Re: Si570 rotary encoder

Yahoo group: PPLL-VFO
Date: 2014-09-22 01:22:10 UTC
From: Craig Johnson, AA0ZZ
Topic: 291 Message: 296

Larry,

Congratulations! You found a way to make it work the way you want it to and that’s perfect.

Your homebrewing projects sound great too.

Good luck in your new pursuits.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Sunday, September 21, 2014 12:25 PM
To: PPLL-VFO@yahoogroups.com
Subject: Re: [PPLL-VFO] Re: Si570 rotary encoder

Hi Craig...

Thanks for the reply.

I sourced a rotary encoder (from work!!) and after a little experimentation, it works! The tuning action is a bit different because the new encoder has detents as you turn it. But I kinda like that! And it means there is no wiggle between digits. This one moves definitely from one rotary position to another.

Thank you for your kind offer. But I'm good now.

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I have had loads of fun with it. But it is too large for serious long haul biking and camping so I am building another one based on FFT with a crystal in the middle of the band and a high speed codec. This one'll be tiny. CW and SSB maybe on 20 meters this time. I hope to have it ready in the spring for biking adventures next year.

73,
Larry. VO1HL

Sent from my ASUS Pad

"aa0zz@... [PPLL-VFO] <mailto:aa0zz@...%20[PPLL-VFO]> " <PPLL-VFO@yahoogroups.com> wrote:

Hi Larry,

There isn't a part number for these encoders that you can use for ordering. I got them by buying a large quantity from China. I agree that they are quite unique in performance compared to normal mechanical encoders.

Please send me your name and address and I will send you one. Might have to charge you something for postage.

Best Regards,

-Craig, AA0ZZ

297. Si5351 VFO frist try

Yahoo group: PPLL-VFO
Date: 2014-10-09 23:41:29 UTC
From: duwayne@...
Topic: 297 Message: 297

I recently saw an add for a small breakout board for a si5351 clock generator from Adafruit. Ordered a couple and started looking for software for it. Found a nice Arduino library by Jason NT7S. Threw together a quick breadboard circuit and yesterday did up a preliminary circuit board. The complete board consists of a Nano ,the Adafruit board, a Nokia display, and a rotary encoder. I built this board with sockets and it is quite deep. After I get everything positioned around a little bit I will do another board and directly solder them to the main board. This should give me something less than 1 in thick. Because of the small display I decided to show the frequency in Khz. in a large font, and the Hz.in a smaller font. this also allowed me to show the step size directly below the Hz. value, and not take up additional display space.
I posted a couple of pictures of the progress so far. After I get a the layout finalized I will post the eagle cad layout. So far this is a single layer board that I did up using toner transfer. Final board should also be 1 sided, with just the display and encoder pins being solder on the bottom.
73
DuWayne KV4QB

298. Re: Si5351 VFO frist try

Yahoo group: PPLL-VFO
Date: 2014-10-10 03:22:34 UTC
From: Shawn Reed
Topic: 297 Message: 298

Hi Duwayne. Check out also, that NT7S has developed a Si5351A breakout board himself, where he added transformers (minicircuits TC1-6X+) , for isolation. "Ripples in the Ether" blog has info to purchase three boards for $15.50 from Osh Park. In Github is a file and schematic of the circuit, with the components labeled. I've got the boards, and the parts on on the way. Only I am still in question on the capacitors. Yet to order. Not sure on the voltage rating to get. I would think maybe 16v, but would 25v or 50v work as well? I would like to check your project out. I don't have one in mind at the moment, but kits and boards come and go, so fast sometimes, I thought I would order and stash the board and parts for the future. Have a good day, Shawn. KF7YFF.

299. Re: [PPLL-VFO] Re: Si5351 VFO frist try

Yahoo group: PPLL-VFO
Date: 2014-10-10 03:43:57 UTC
From: DuWayne KV4QB
Topic: 297 Message: 299

Yes I found that out after I ordered the boards form Adafruit. I stuck with those after adding up what it would cost to piece it all out. The ones from Adafruit are $7.95 and come assembled, and are a little smaller. I have ordered several boards some of my design and some other designs from OSH Park, and have been happy with them. If I need the isolated output I can always add it to the circuit I will be driving. 16v. should be fine for the circuit, only running on5 v. in and 3.3 v for the si5351 itself. When I get it finished I will post the eagle cad file and Arduino sketch. You should be able to send to OSH Park and have them made. Size is about 2 x 3.25 inches, should cost about $10 per board. One thing I did find when I started to lay the board out, there are 2 different pin outs for the NOKIA LCD displays. Laid first one out with the one I had on hand and when others came in found a different pinout.
Will keep you updated as I go along. So far it is a nice little project. Since there are 3 clocks on board, thinking of a general coverage receiver. First If 45 Mhz. to avoid images then a 9 Mhz. 2nd.
73 DuWayne KV4QB

On 10/9/2014 11:22 PM, Shawn Reed sreedq1014@... [PPLL-VFO] wrote:
> Hi Duwayne. Check out also, that NT7S has developed a Si5351A breakout
> board himself, where he added transformers (minicircuits TC1-6X+) ,
> for isolation. "Ripples in the Ether" blog has info to purchase three
> boards for $15.50 from Osh Park. In Github is a file and schematic of
> the circuit, with the components labeled. I've got the boards, and the
> parts on on the way. Only I am still in question on the capacitors.
> Yet to order. Not sure on the voltage rating to get. I would think
> maybe 16v, but would 25v or 50v work as well? I would like to check
> your project out. I don't have one in mind at the moment, but kits and
> boards come and go, so fast sometimes, I thought I would order and
> stash the board and parts for the future. Have a good day, Shawn. KF7YFF.
>

--
Of all the things I lost, I miss my mind the most.

300. New file uploaded to PPLL-VFO

Yahoo group: PPLL-VFO
Date: 2014-12-23 14:25:49 UTC
From: PPLL-VFO@yahoogroups.com
Topic: 216 Message: 300

Hello,

This email message is a notification to let you know that
a file has been uploaded to the Files area of the PPLL-VFO
group.

File : /AA0ZZ - PIC-EL FreqCounter/PECntr28g.HEX
Uploaded by : aa0zz <aa0zz@...>
Description : PIC code for Freq Counter v2.8g 1/13/2007

You can access this file at the URL:
https://groups.yahoo.com/neo/groups/PPLL-VFO/files/AA0ZZ%20-%20PIC-EL%20FreqCounter/PECntr28g.HEX

To learn more about file sharing for your group, please visit:
https://help.yahoo.com/kb/index?page=content&y=PROD_GRPS&locale=en_US&id=SLN15398

Regards,

aa0zz <aa0zz@...>

301. VFO's, LNA FS

Yahoo group: PPLL-VFO
Date: 2015-02-03 17:03:03 UTC
From: ai1g@...
Topic: 301 Message: 301

All,
I have the following items for sell. All professionally built, tested by me. All boards ready to be mounted in the enclosure of your choice. I did build one PCB enclosure for the IQ PRO but never got to mount the boards. I have some health issues that will not allow me to build my own radios anymore. I know Craig and he knows I am posting these here. The IQPRO makes a great VFO for the R2Pro or any Quadrature based VFO/Xmitter.

Contact me at ai1g@...
Pay via Paypal (guy@...) or personal check.

SI570 Daughter Card and Controller board $65.00
Built/Tested IQPRO Quadrature VFO $200.00

Built LNA/LPF for IQPRO (or other VFO) $75.00

best regards; (73)

Guy Mengel AI1G

302. 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-09 13:04:56 UTC
From: gpatterson53@...
Topic: 302 Message: 302

anyone done this on 10 meters. i have built one with a high speed 74actq74sc. it is unstable above 28.5 mhz. any ideas?

303. Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 00:04:08 UTC
From: Nick Kennedy
Topic: 302 Message: 303

I just finished or am finishing such a receiver. I did one brief test on 10 meters just to verify I could hear a signal, but nothing extensive enough to say it would work up to the top of the band.

I used 74AC flip-flops.

73-

Nick, WA5BDU

On Sat, Apr 9, 2016 at 8:04 AM, gpatterson53@...m [PPLL-VFO] <PPLL-VFO@yahoogroups.com> wrote:

>
>
> anyone done this on 10 meters. i have built one with a high speed
> 74actq74sc. it is unstable above 28.5 mhz. any ideas?
>
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304. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 00:39:27 UTC
From: Craig Johnson, AA0ZZ
Topic: 302 Message: 304

Hi Guys,

I suspect that the Si570 signal amplitude at 28 MHz has decreased a bit and is no longer enough to reliably trigger the Flip Flop. In fact, if you look closely at the 74AC74 spec sheet, the 1.5v p-p output of the Si570 even at lower frequencies may not meet the specs.

I always condition the signal coming out of the Si570 before feeding it into the divide-by-four 74AC74 FFs. An amplifier would work but I use a couple of XOR gates, set up such that they trigger right in the middle of the range. Then the output of the XOR gates is a full 5v p-p.

I learned about this XOR trick from Don Huff, W6JL, and did a write-up on it. I just posted the write-up in the FILES section. It's called

" <https://xa.yimg.com/df/PPLL-VFO/W6JL+trick+using+XOR+gates+to+drive+flipflops.docx?token=XB9RHLYnucrPB2rT3bS7oYsoDZaXL26okeaqEE0UjdVRz_ME69bXuJ0CeWIDFsL8TcLTTwRjKcpz-PuNBmqlHvs1Kf7-gKL38UZjIpHWGbgOgtsmo1N1wfKMpChiPP1kni5oIFCsv0S026mgph0--jM1_48-E_Yye3yxeC2zOg&type=download> W6JL trick using XOR gates to drive flipflops.docx"

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Saturday, April 09, 2016 7:04 PM
To: PPLL-VFO@yahoogroups.com
Subject: Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

I just finished or am finishing such a receiver. I did one brief test on 10 meters just to verify I could hear a signal, but nothing extensive enough to say it would work up to the top of the band.

I used 74AC flip-flops.

73-

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305. Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 01:28:32 UTC
From: Nick Kennedy
Topic: 302 Message: 305

Craig,

I tried that "center finding" circuit but it gave me a lot of trouble because it draws a heck of a lot of current. So in a later version I did away with it and drove a 3.3 V 74AC74 directly from the Si570, but used a voltage divider to shift it back to 0 to 3.3 volts from the +/- 1.65 V I have coming out of the Si570 box.

73-

Nick, WA5BDU

On Sat, Apr 9, 2016 at 7:39 PM, 'Craig Johnson, AA0ZZ' aa0zz@... [PPLL-VFO] <PPLL-VFO@yahoogroups.com> wrote:

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> Hi Guys,
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> and is no longer enough to reliably trigger the Flip Flop. In fact, if you
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> the range. Then the output of the XOR gates is a full 5v p-p.
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> “*W6JL trick using XOR gates to drive flipflops.docx*
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> ”
>
> Best Regards,
>
> -Craig, AA0ZZ
>
>
>
> *From:* PPLL-VFO@...m [mailto:PPLL-VFO@yahoogroups.com]

> *Sent:* Saturday, April 09, 2016 7:04 PM
> *To:* PPLL-VFO@yahoogroups.com
> *Subject:* Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570
>
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>
> I just finished or am finishing such a receiver. I did one brief test on
> 10 meters just to verify I could hear a signal, but nothing extensive
> enough to say it would work up to the top of the band.
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> I used 74AC flip-flops.
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> 73-
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306. Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 02:49:19 UTC
From: aa0zz@...
Topic: 302 Message: 306

Hi Nick, Yes, if you are current limited it may be a problem. I haven't had that issue soi it's worked for me.
Your 3v solution sounds like another way to go.
73,
-Craig

307. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 12:37:28 UTC
From: Pierre Drolet
Topic: 302 Message: 307

Hi Craig,

My name is Pierre Drolet and I used to be a member of this group until Yahoo cancelled my account!!!

Can you please reset this to pdrolet22@....

Thanks for your help and maintaining this group.

Pierre

VE2DID

De : PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Envoyé : 9 avril 2016 20:39
À : PPLL-VFO@yahoogroups.com
Objet : RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Hi Guys,

I suspect that the Si570 signal amplitude at 28 MHz has decreased a bit and is no longer enough to reliably trigger the Flip Flop. In fact, if you look closely at the 74AC74 spec sheet, the 1.5v p-p output of the Si570 even at lower frequencies may not meet the specs.

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Best Regards,

-Craig, AA0ZZ

From: <mailto:PPLL-VFO@yahoogroups.com> PPLL-VFO@yahoogroups.com [<mailto:PPLL-VFO@yahoogroups.com> mailto:PPLL-VFO@yahoogroups.com]
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To: <mailto:PPLL-VFO@yahoogroups.com> PPLL-VFO@yahoogroups.com
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I used 74AC flip-flops.

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No virus found in this message.
Checked by AVG - www.avg.com
Version: 2016.0.7538 / Virus Database: 4545/12003 - Release Date: 04/10/16

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Checked by AVG - www.avg.com
Version: 2016.0.7538 / Virus Database: 4545/12003 - Release Date: 04/10/16

308. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 14:23:27 UTC
From: gpatterson53@...
Topic: 302 Message: 308

craig:

i have trouble understanding how the XOR gate "trick" works on 28 mhz. the xor's, as i recall max out at 55mhz and the 4 x si570 on 10 meters is 112 mhz

309. Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 15:10:19 UTC
From: Nick Kennedy
Topic: 302 Message: 309

Craig's receiver in the QEX article was 40 meters only. However, W6JL uses the same chip and I was under the assumption he ran all HF bands with it. Looking through the PDF of his design description though, I don't see that claim.

I'd probably go ahead with a faster rated chip. It's interesting though that the circuit runs as an oscillator if there's no drive and still does its job of finding the center point.

73-

Nick, WA5BDU

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> 112 mhz
>
>
>

310. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 16:49:23 UTC
From: Craig Johnson, AA0ZZ
Topic: 302 Message: 310

I just looked at the spec sheet for the 74AC74 that I am using and see that the max clock frequency is 95 MHz. This would be a problem for 10 Meters (30 MHz).

The spec for the 74AC74 says when running at 3v needs at least 2.1v for a reliable high and below 0.9v for a reliable low. If the Si570's 1.5v p-p signal is biased in the middle of this range (i.e, at 1.5v) then the and minus 0.75 volts from the SI570 would work without the XOR gates.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Saturday, April 09, 2016 7:39 PM
To: PPLL-VFO@yahoogroups.com
Subject: RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Hi Guys,

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311. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-10 16:50:44 UTC
From: Craig Johnson, AA0ZZ
Topic: 302 Message: 311

Hi Pierre,

I have no idea what happened.

Try the “JOIN” again and identify yourself and I will approve.

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Sunday, April 10, 2016 7:37 AM
To: PPLL-VFO@yahoogroups.com
Subject: RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Hi Craig,

My name is Pierre Drolet and I used to be a member of this group until Yahoo cancelled my account!!!

Can you please reset this to pdrolet22@....

Thanks for your help and maintaining this group.

Pierre

VE2DID

De : PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Envoyé : 9 avril 2016 20:39
À : PPLL-VFO@yahoogroups.com
Objet : RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

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Version: 2016.0.7538 / Virus Database: 4545/12003 - Release Date: 04/10/16

312. RE: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-11 02:01:04 UTC
From: Craig Johnson, AA0ZZ
Topic: 302 Message: 312

Actually, my the code for the Si570 boards that were described in my QEX article was a “building block” that went up to 156 MHz. I had an example for a 40 Meter receiver and also some transmitter ideas but it really left it up to the user to figure out how to use it.

I was looking at the spec sheet for another 74AC74 part by Fairchild and the maximum frequency when run at 5v is at least 140 MHz and typically160 MHz. A t 3.3v it’s at least 100 MHz and typically 125 MHz.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Sunday, April 10, 2016 10:10 AM
To: PPLL-VFO@yahoogroups.com
Subject: Re: [PPLL-VFO] 10 meter tayloe mixer 4 x si570

Craig's receiver in the QEX article was 40 meters only. However, W6JL uses the same chip and I was under the assumption he ran all HF bands with it. Looking through the PDF of his design description though, I don't see that claim.

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313. Re: 10 meter tayloe mixer 4 x si570

Yahoo group: PPLL-VFO
Date: 2016-04-11 03:45:10 UTC
From: gpatterson53@...
Topic: 302 Message: 313

yes ....i just rebuilt my tayloe with the 74actq74 running at 3.3v. biased the si570 output and now all works well through 30mhz. thanks for all the replies. gary

314. Mini Computers

Yahoo group: PPLL-VFO
Date: 2016-04-27 19:49:20 UTC
From: <serracin7388@...>
Topic: 314 Message: 314

blockquote, div.yahoo_quoted { margin-left: 0 !important; border-left:1px #715FFA solid !important; padding-left:1ex !important; background-color:white !important; } Anyone used SDR with Raspberry PI ?

Sent from Yahoo Mail for iPad

315. Re: [PPLL-VFO] Mini Computers

Yahoo group: PPLL-VFO
Date: 2016-04-28 10:40:05 UTC
From: John
Topic: 314 Message: 315

Yes several people have used it with their Softrock SDR
https://groups.yahoo.com/neo/groups/softrock40/

John

From: mailto:PPLL-VFO@yahoogroups.com
Sent: Wednesday, April 27, 2016 8:49 PM
To: yahoogroups
Subject: [PPLL-VFO] Mini Computers

Anyone used SDR with Raspberry PI ?

316. ZZRX-40

Yahoo group: PPLL-VFO
Date: 2016-08-14 20:15:24 UTC
From: Granville Howerton
Topic: 316 Message: 316

What is the plug size of the ear bud?What is the antenna plug size?

Thx

Gary H.

317. RE: [PPLL-VFO] ZZRX-40

Yahoo group: PPLL-VFO
Date: 2016-08-14 20:27:13 UTC
From: Craig Johnson, AA0ZZ
Topic: 316 Message: 317

Hi Gary,

It’s a standard 1/8” (3.5mm) jack. It’s part number CP1-3513-ND at DigiKey.

If you have additional questions regarding the ZZRX-40, it would be better to ask them in the ZZRX-40 YAHOO group.

Best Regards,

-Craig, AA0ZZ

From: PPLL-VFO@yahoogroups.com [mailto:PPLL-VFO@yahoogroups.com]
Sent: Sunday, August 14, 2016 3:15 PM
To: PPLL-VFO@yahoogroups.com
Subject: [PPLL-VFO] ZZRX-40

What is the plug size of the ear bud?What is the antenna plug size?

Thx

Gary H.

318. different stuff

Yahoo group: PPLL-VFO
Date: 2016-10-10 00:24:56 UTC
From: Page G
Topic: 318 Message: 318
Attachments: 1 described; binary payloads are missing from this source WARC

Hi,

I've found a lot of interesting stuff that you might like, just take a look
<http://point.sunglossmarblecompany.com/lnbzmgqc>

Warm regards, Page G

319. 74AC74 configuration

Yahoo group: PPLL-VFO
Date: 2018-06-15 19:09:54 UTC
From: pawlud@...
Topic: 319 Message: 319

Can a 74AC74 flip flop be configured to square a fundamental (no division) with 0 and 180 degrees out!

320. Re: 74AC74 configuration

Yahoo group: PPLL-VFO
Date: 2018-06-16 21:42:00 UTC
From: ag4qc@...
Topic: 319 Message: 320

A flip-flop will divide by 2 as that's its main purpose in life. Now it's output's of "Q" and "not Q" will be 180 degrees out of phase but at half the input frequency. If all you want is something that is 180 degrees out of phase, that smells like an inverter. That can be as simple as a simple transistor and a pull-up resistor. Or a 7404 or such IC. If you are trying to square up a signal, a smitt trigger might meet your requirements followed b an inverter. and on and on.

Joe Loucka AG4QC

321. Re: 74AC74 configuration

Yahoo group: PPLL-VFO
Date: 2018-06-16 22:14:32 UTC
From: Bob G3OOU
Topic: 319 Message: 321

It is possible to use a flip-flop as a schmidt trigger by only driving one side of it but although the output waveform is rectangular there is no guarantee that it will be exactly square i.e. 1:1 mark space ratio. I have successfully implemented this technique using fast discrete devices and ECL NOR gates up to at least 200MHz but never with a fully integrated flip-flop.

--
73

Bob

Bob F Burns G3OOU, G-QRP 6907, @BobFBurns
Crystal Palace Radio & Electronics Club: http://cprec.btck.co.uk/
Technical web site: www.qsl.net/g3oou

322. Re: 74AC74 configuration

Yahoo group: PPLL-VFO
Date: 2018-06-18 02:55:56 UTC
From: pawlud@...
Topic: 319 Message: 322

Thanks

323. IQ tests

Yahoo group: PPLL-VFO
Date: 2018-06-18 02:57:40 UTC
From: pawlud@...
Topic: 323 Message: 323

Need to homebrew, or buy, an oscillator, with Quadrature output to test IQ phasings.
Haven’t seen any around!